

FIG. 1
PRIOR-ART

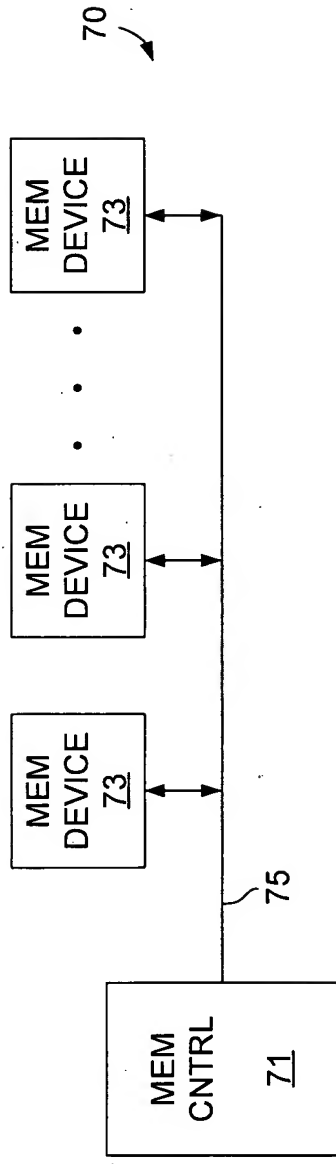
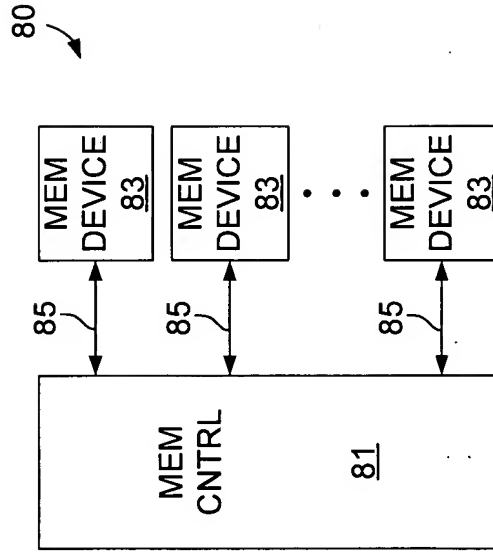


FIG. 2
PRIOR-ART



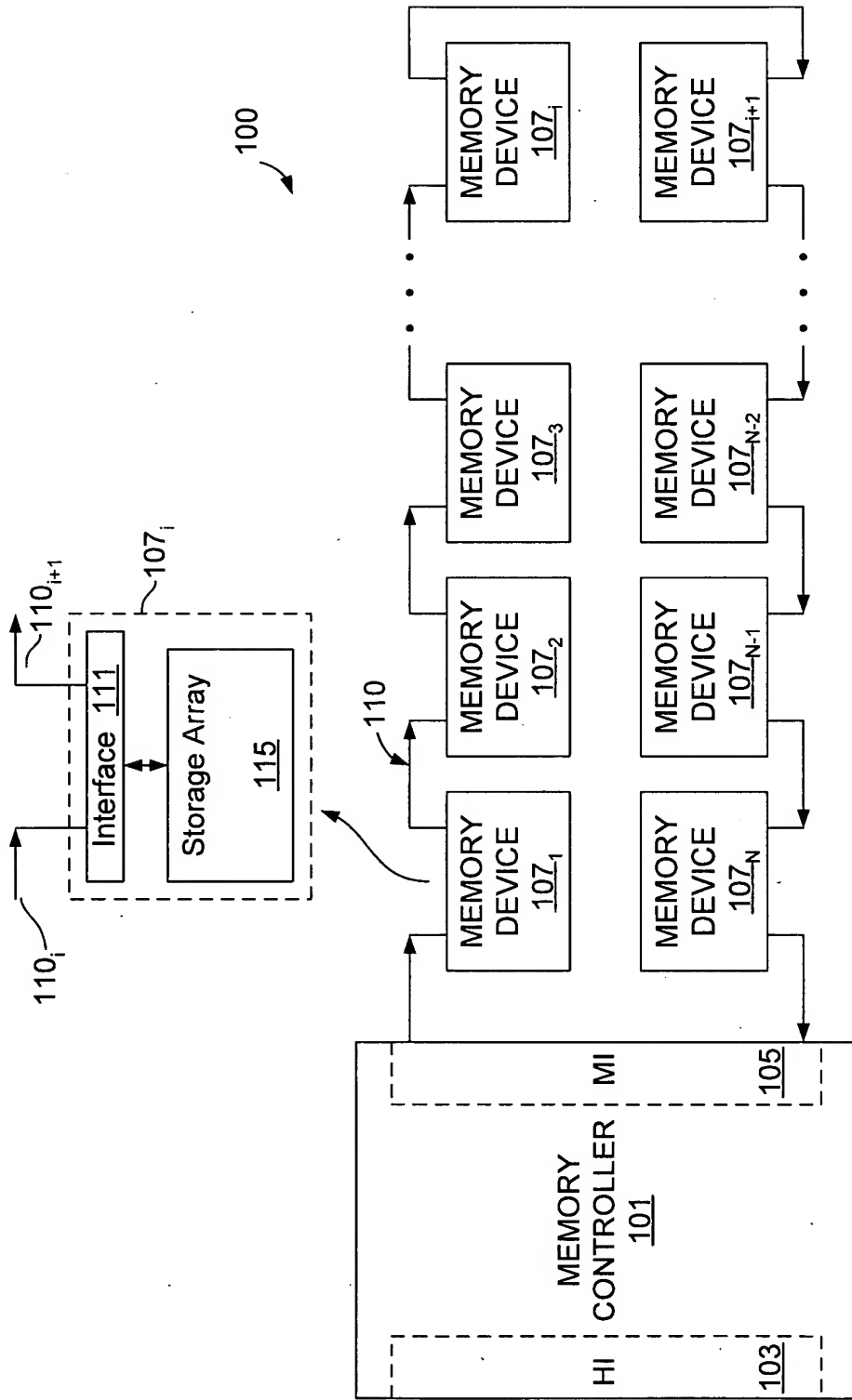


FIG. 3

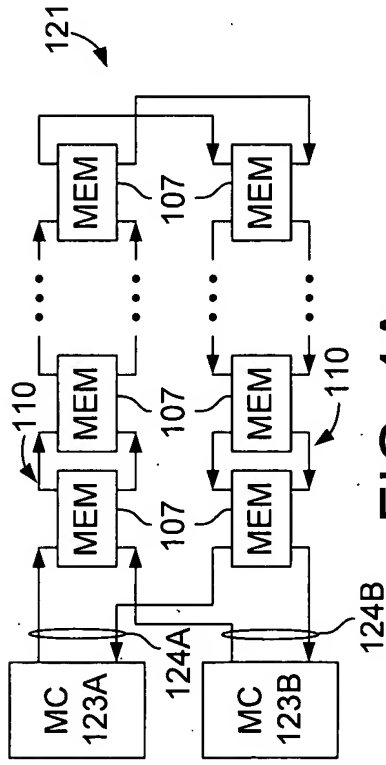


FIG. 4A

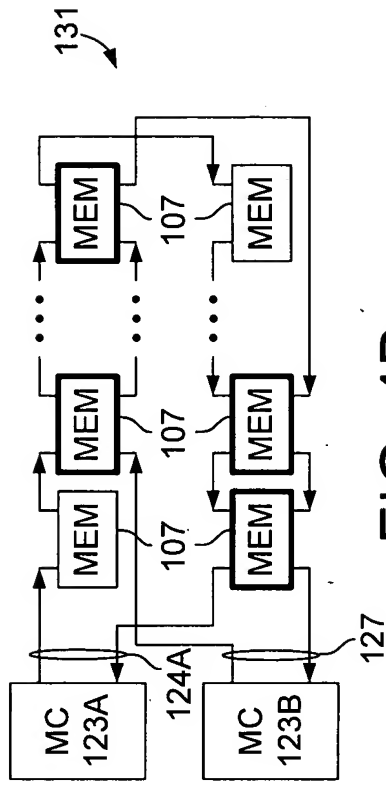


FIG. 4B

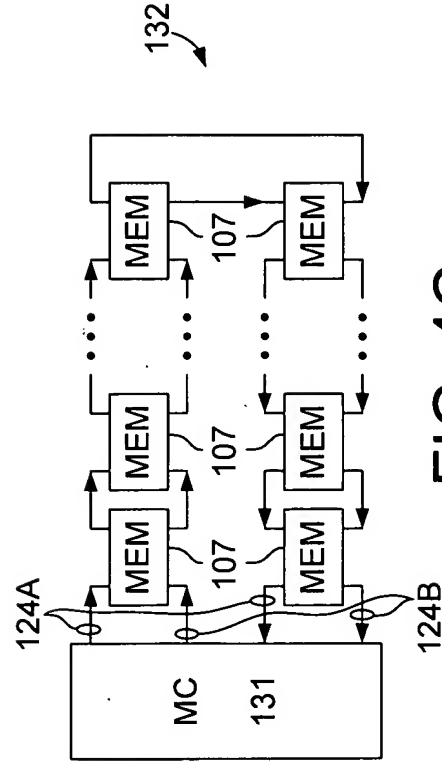


FIG. 4C

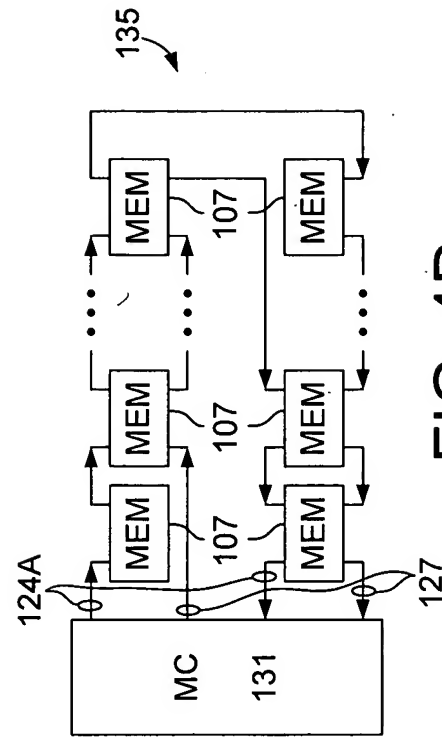


FIG. 4D

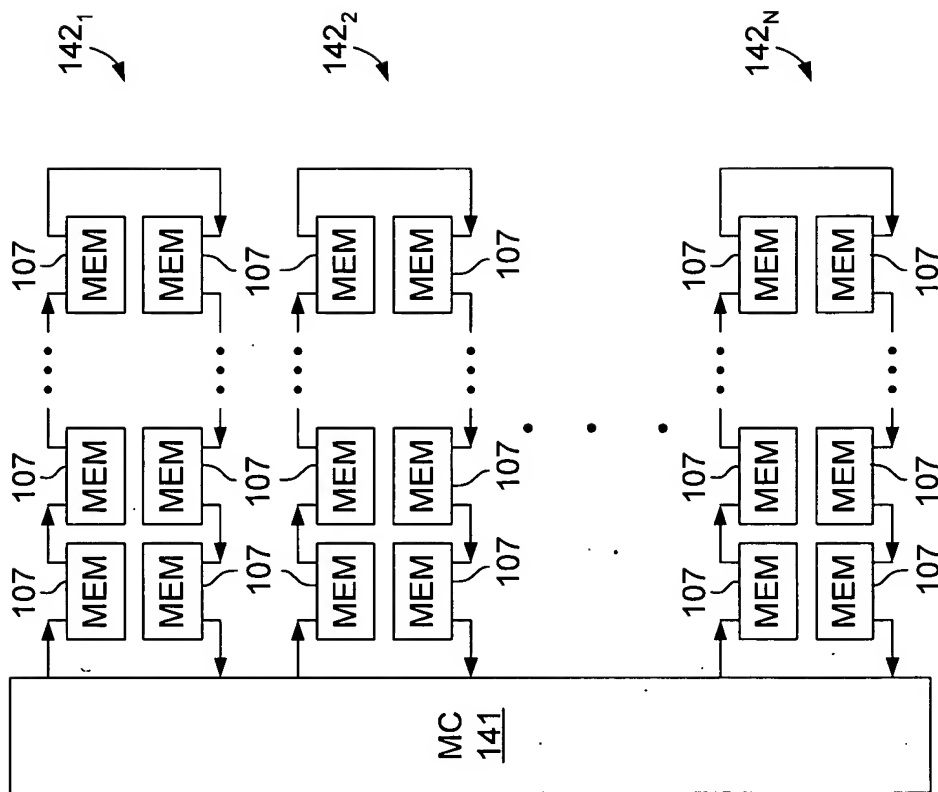


FIG. 4E

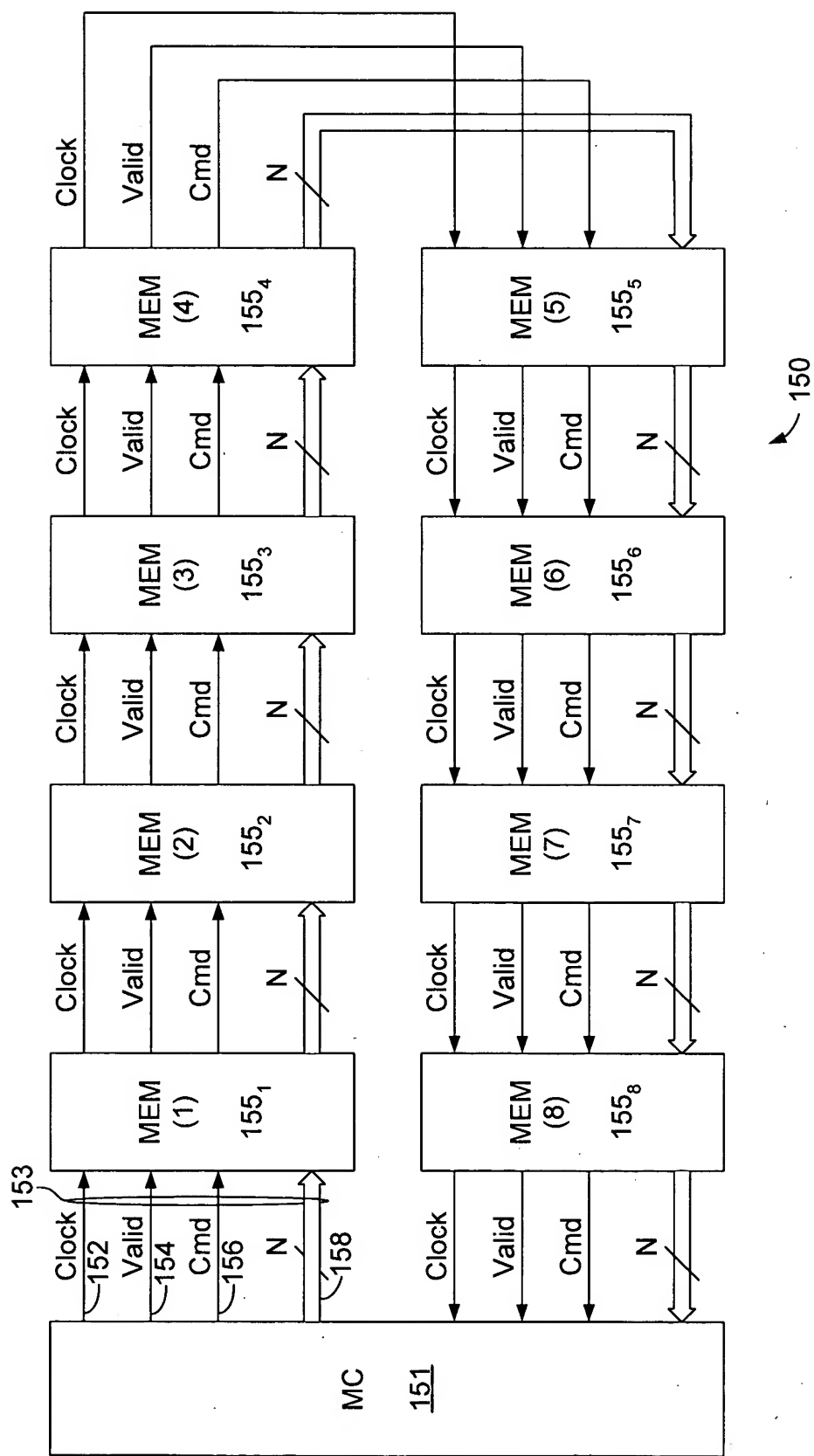


FIG. 5A

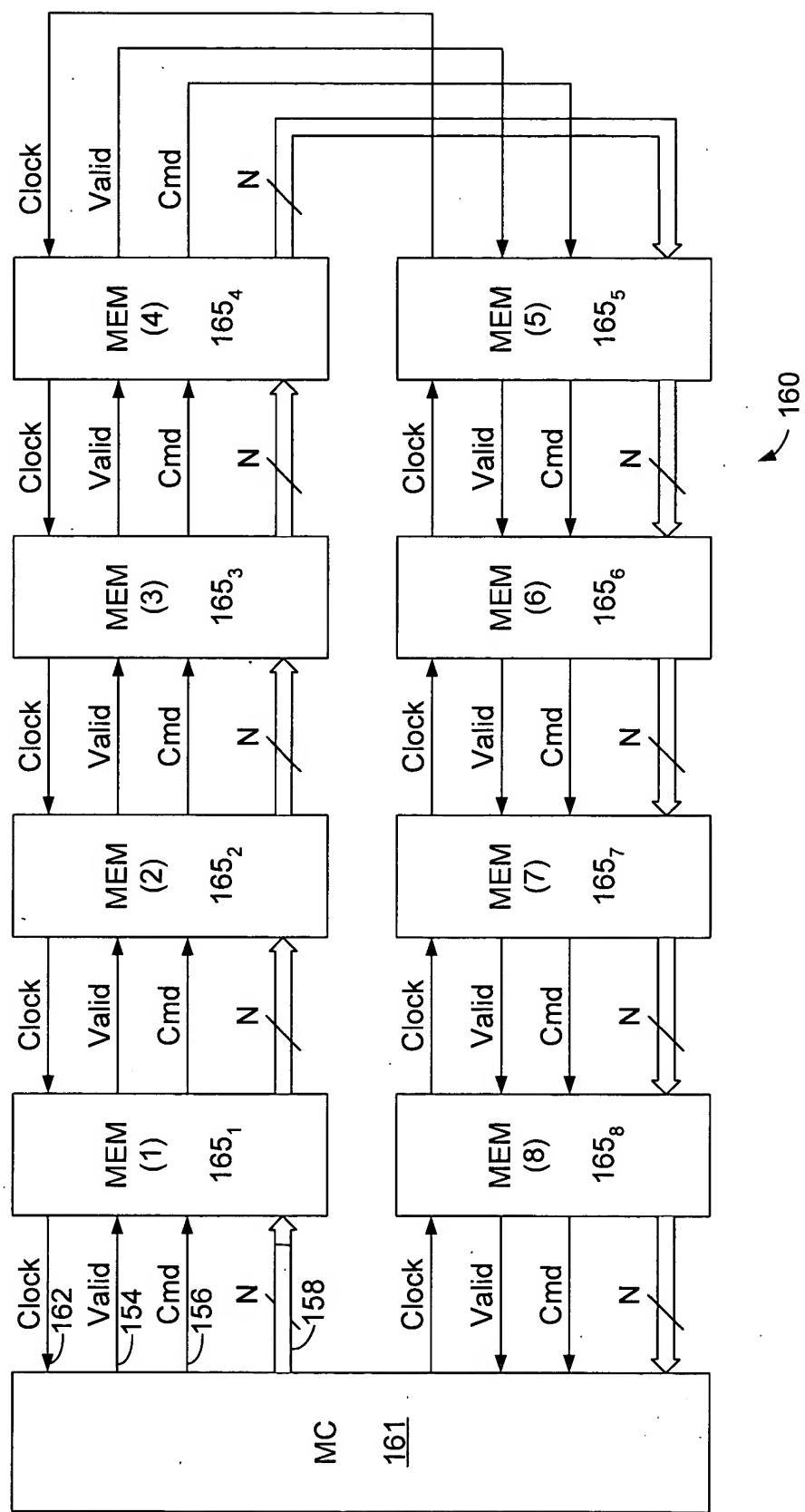


FIG. 5B

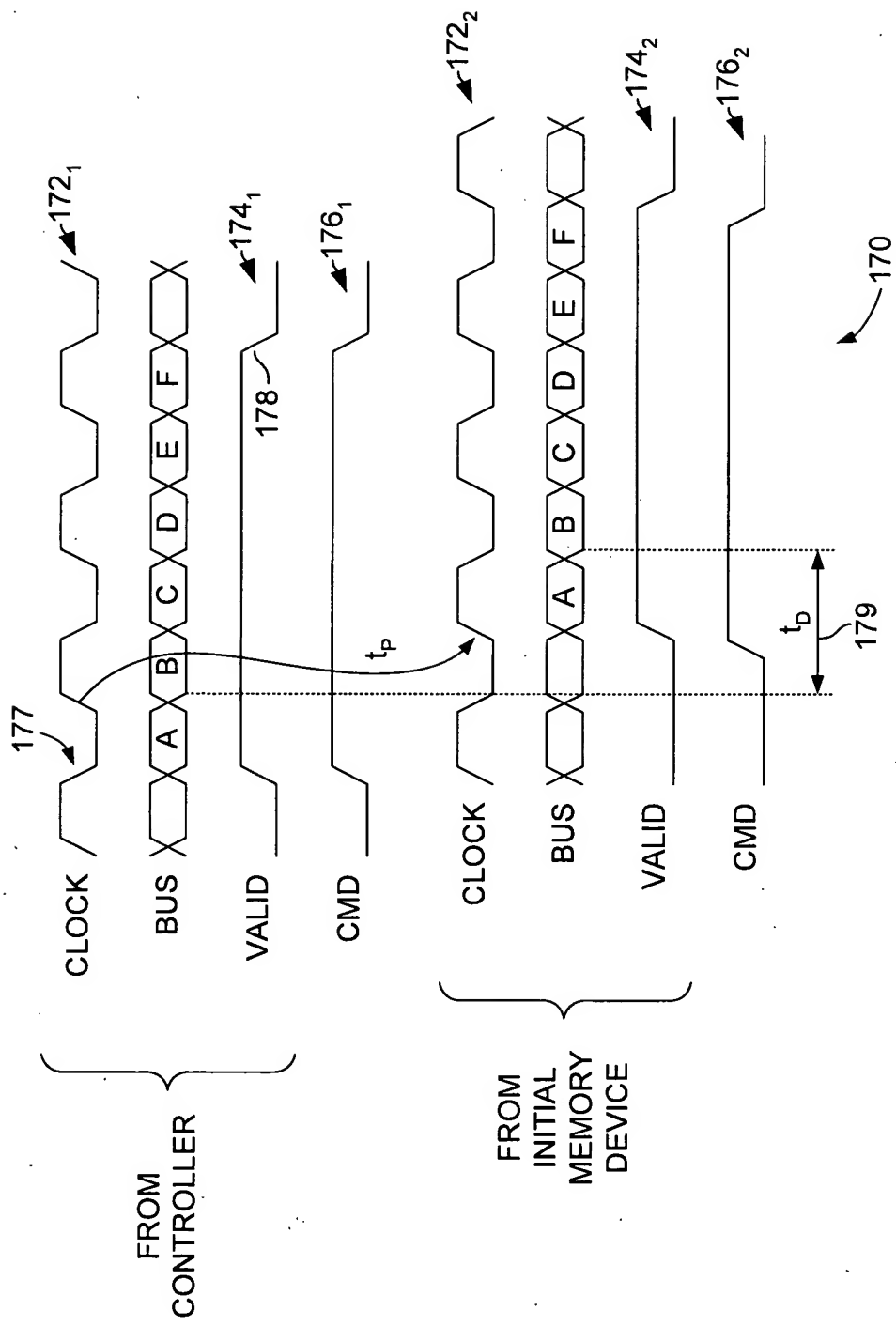


FIG. 6

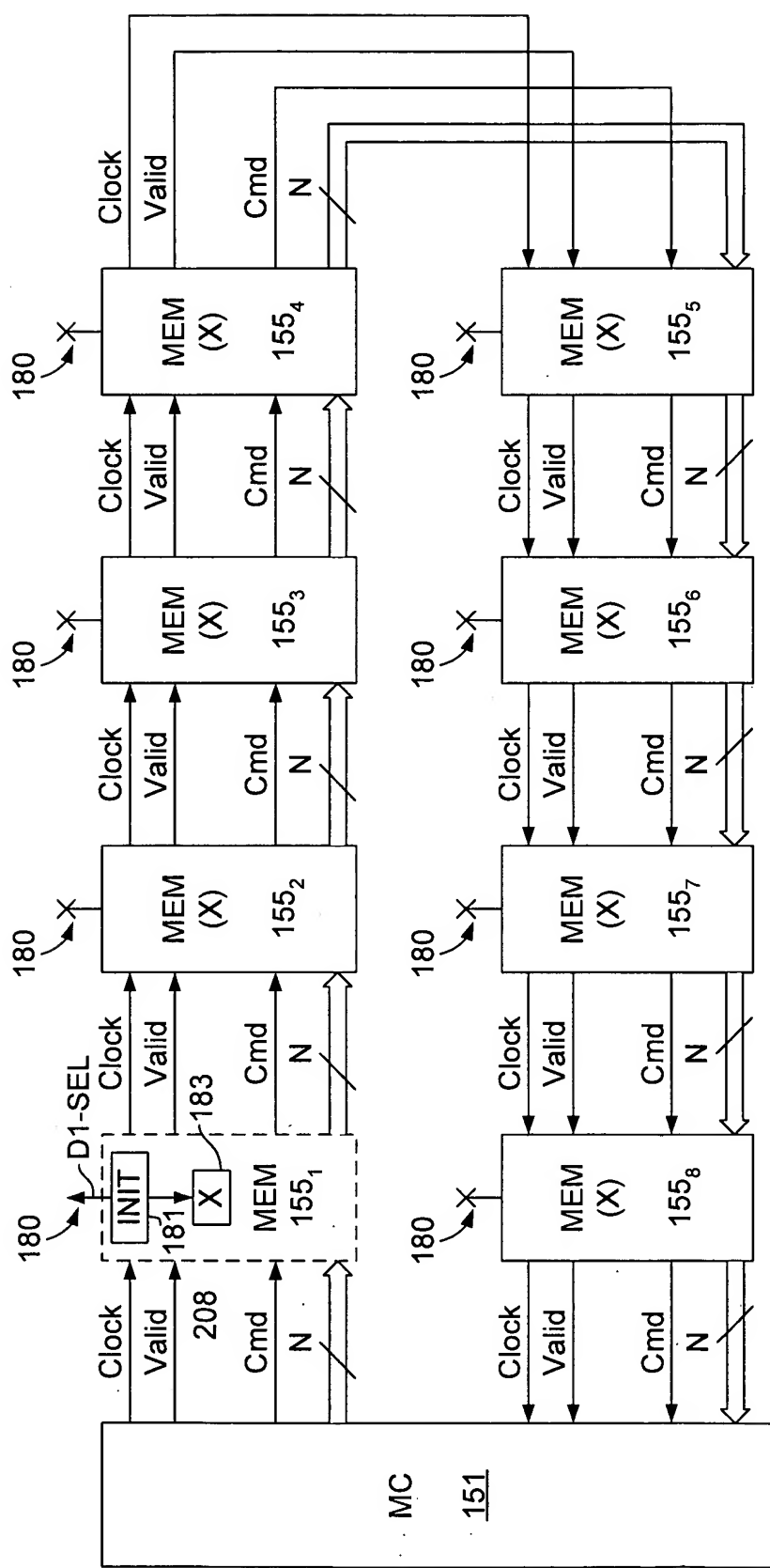


FIG. 7A

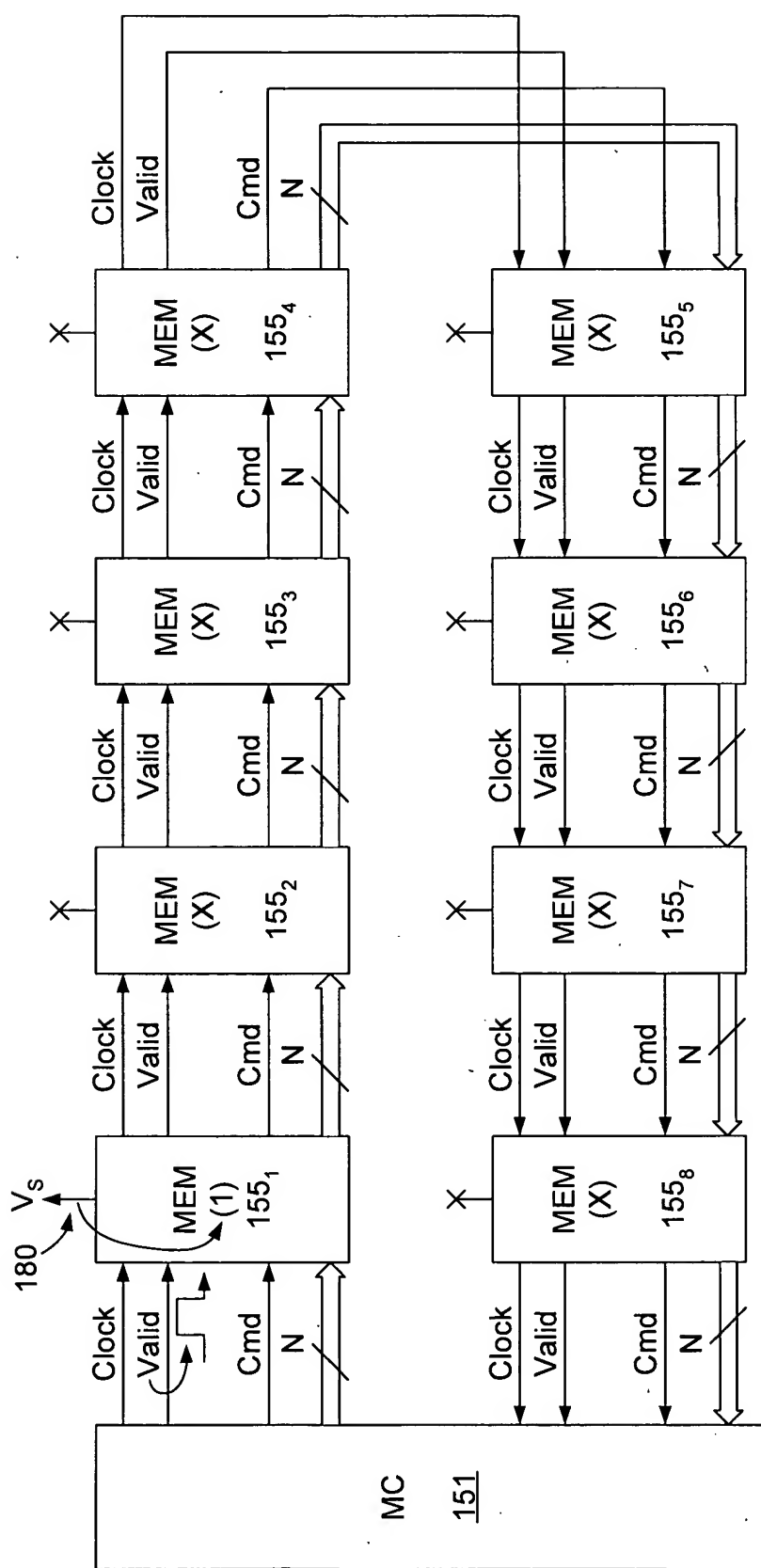


FIG. 7B

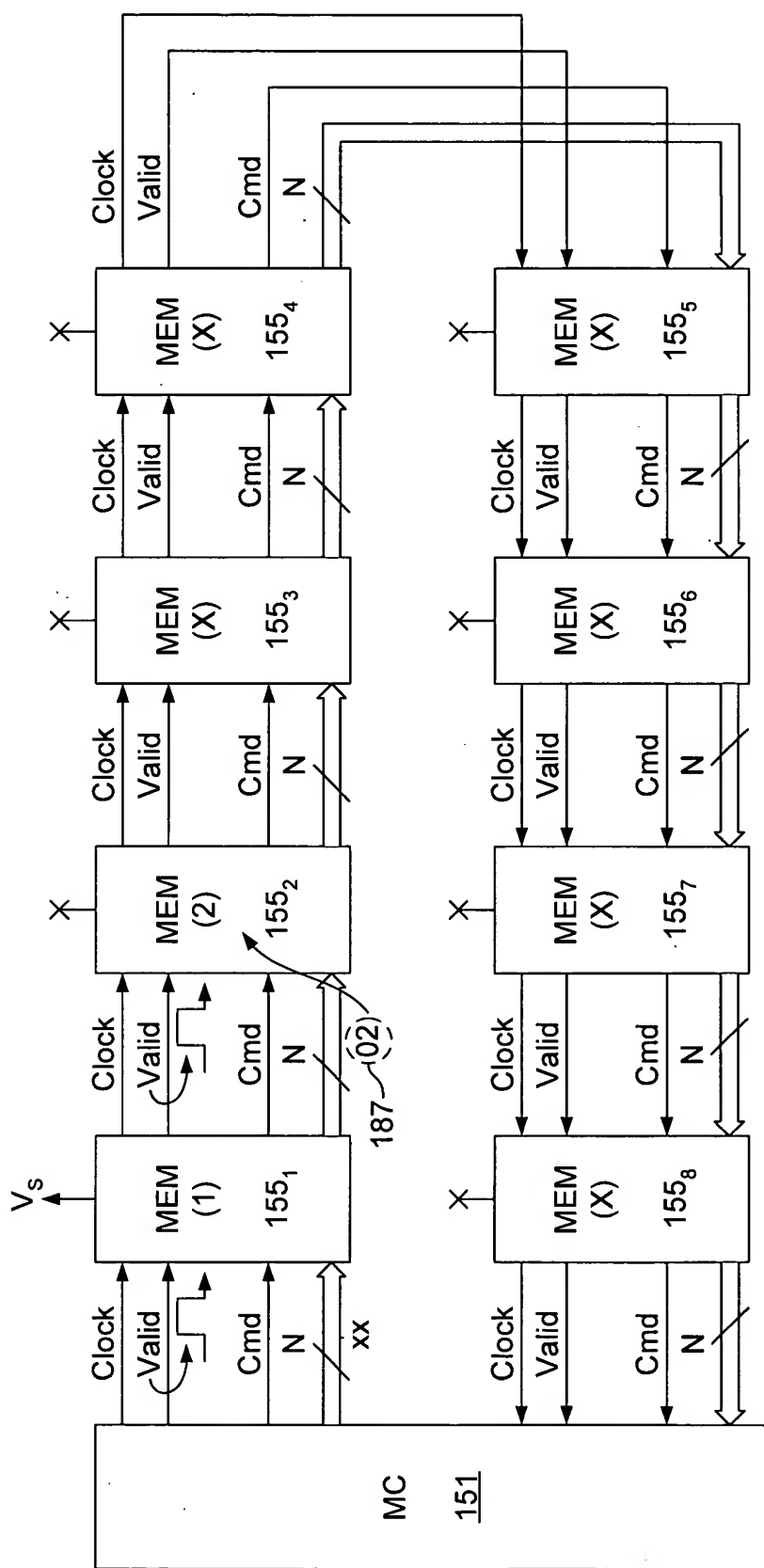


FIG. 7C

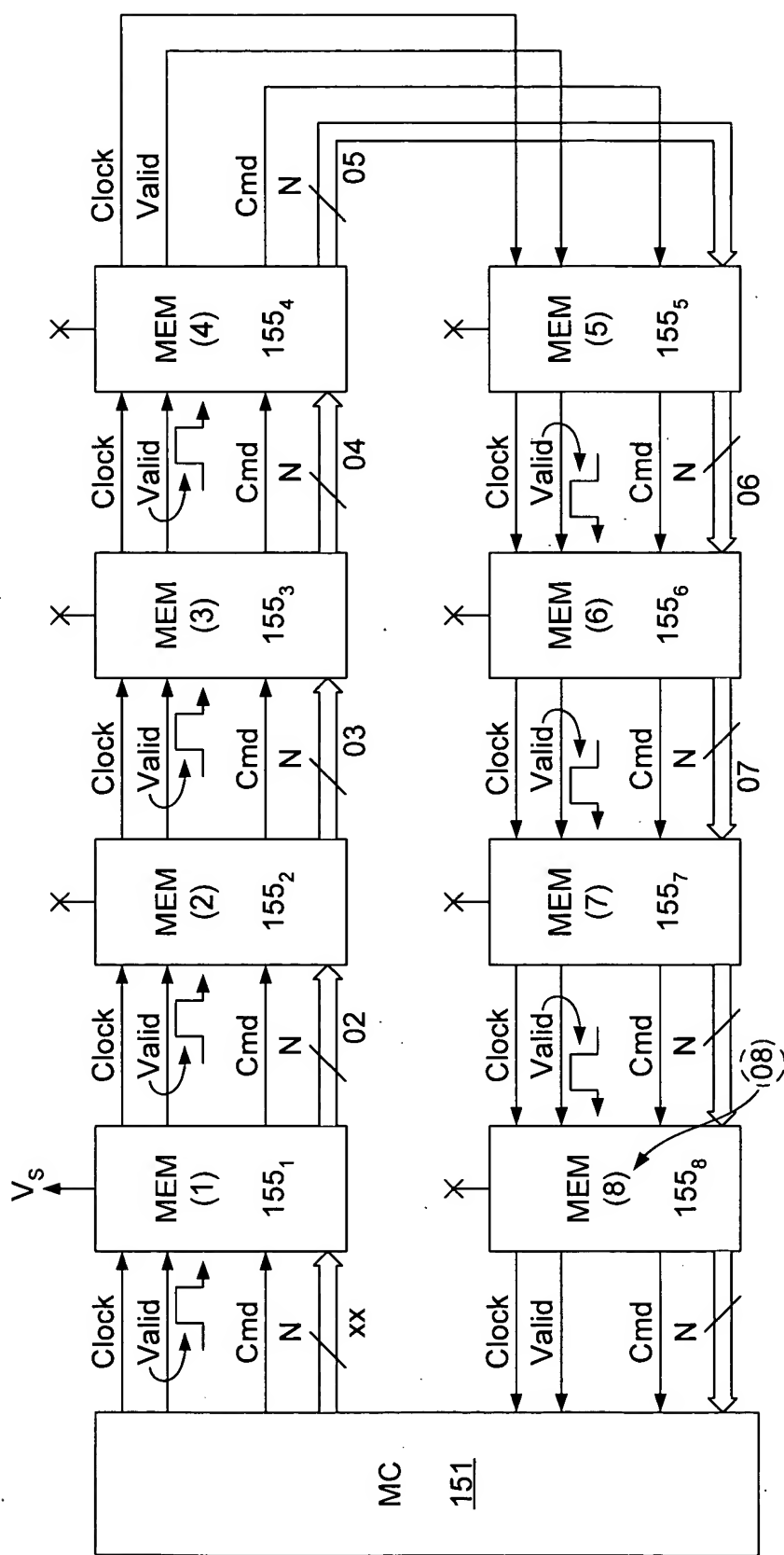


FIG. 7D

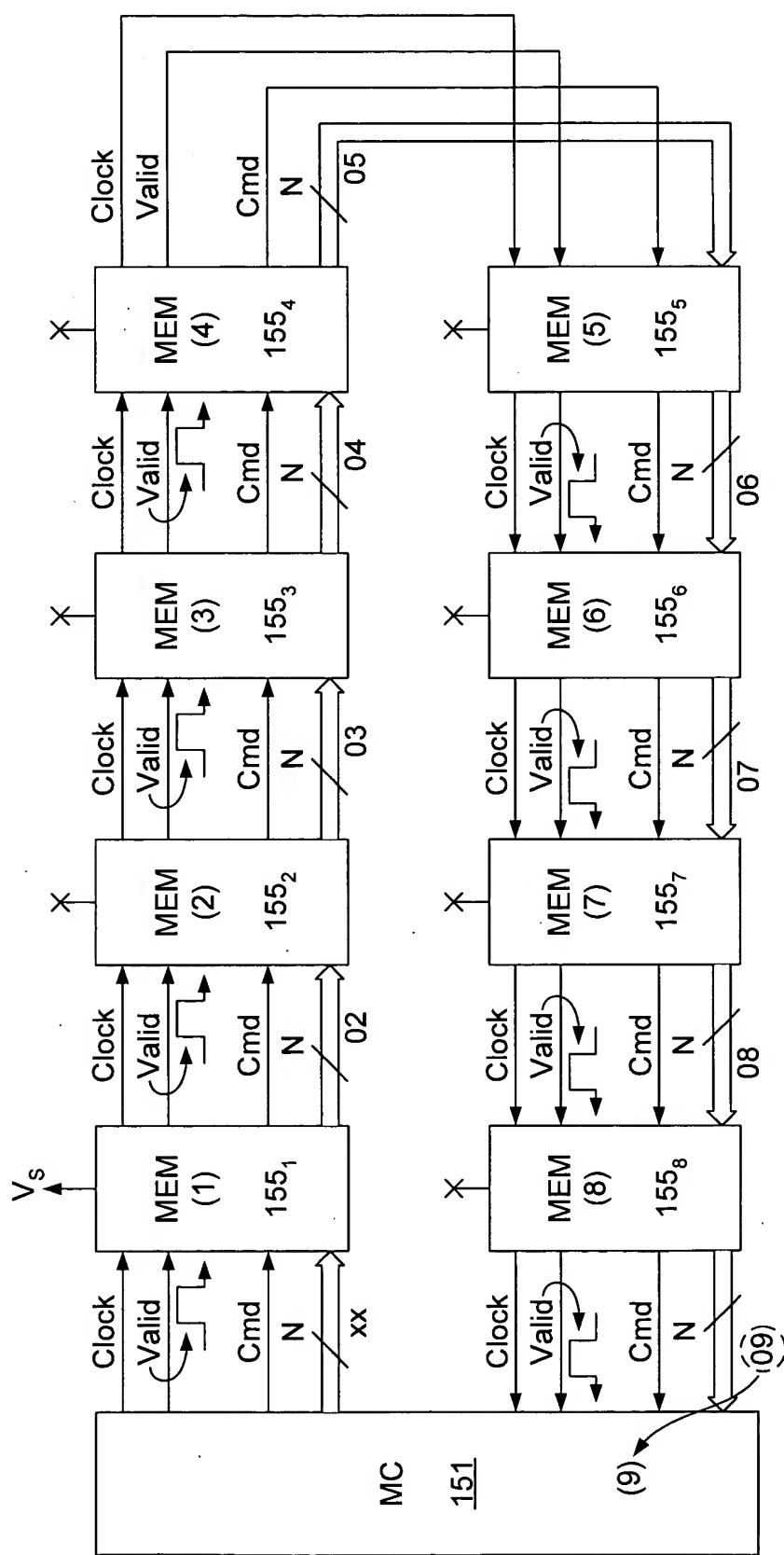
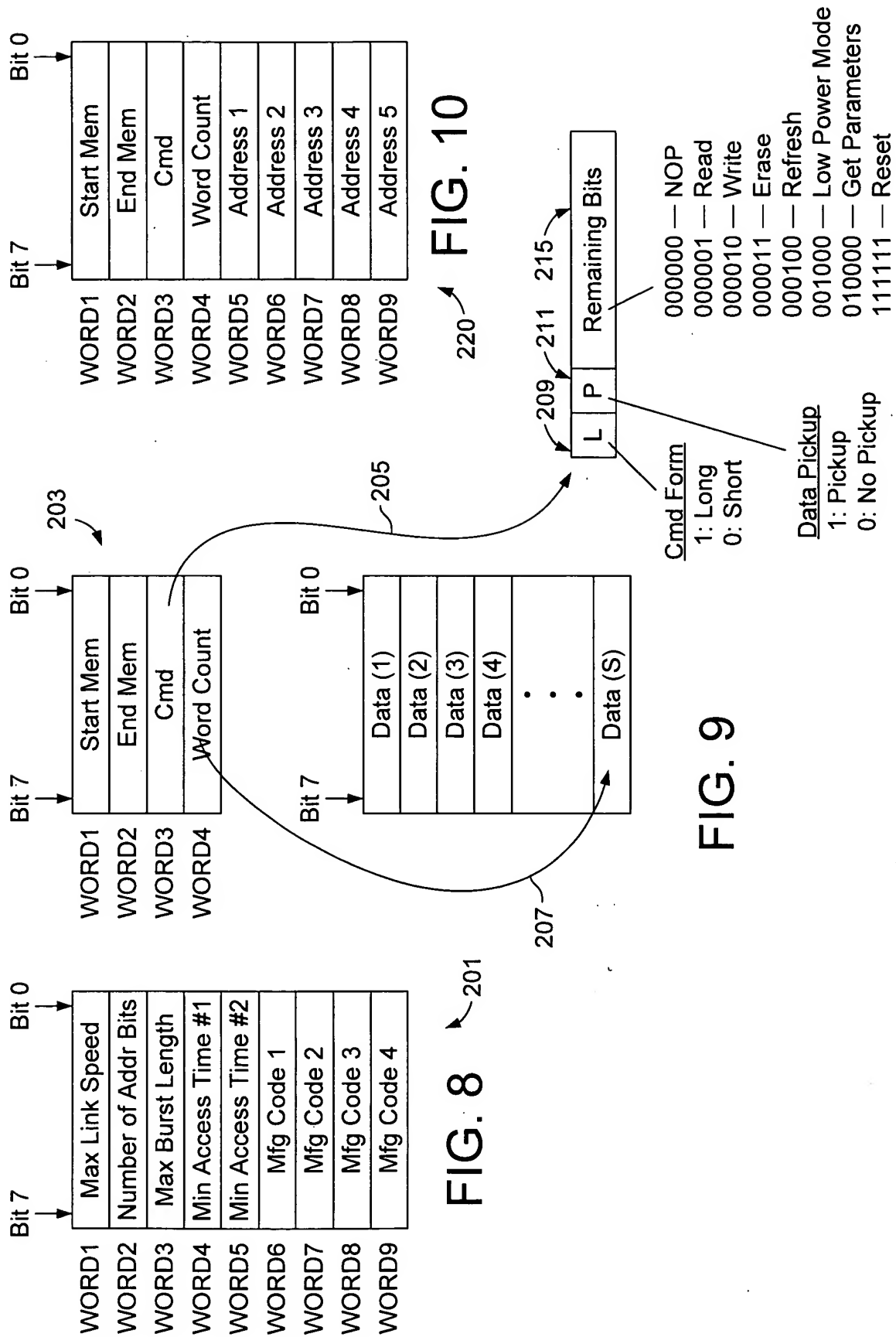


FIG. 7E



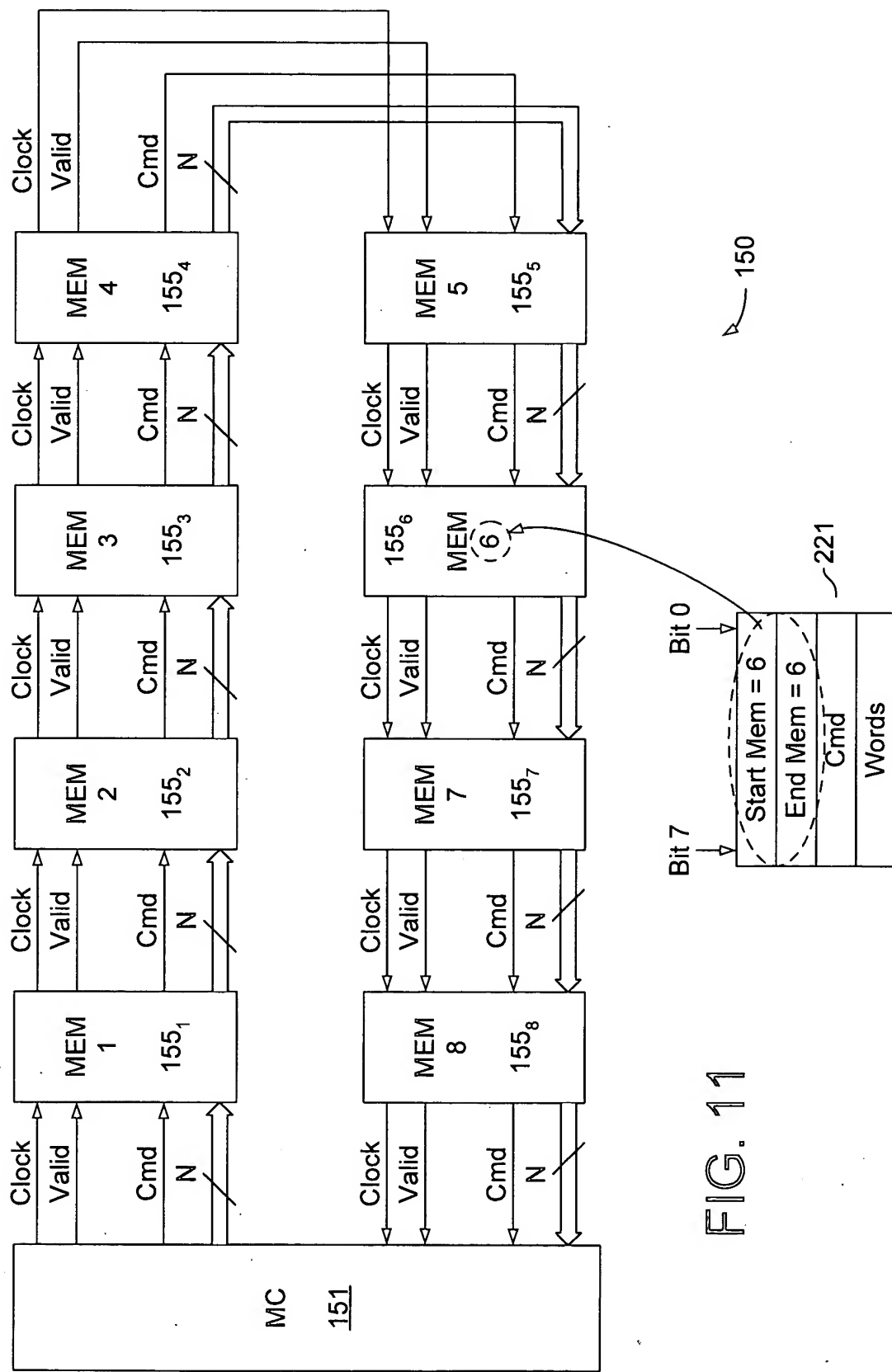


FIG. 11

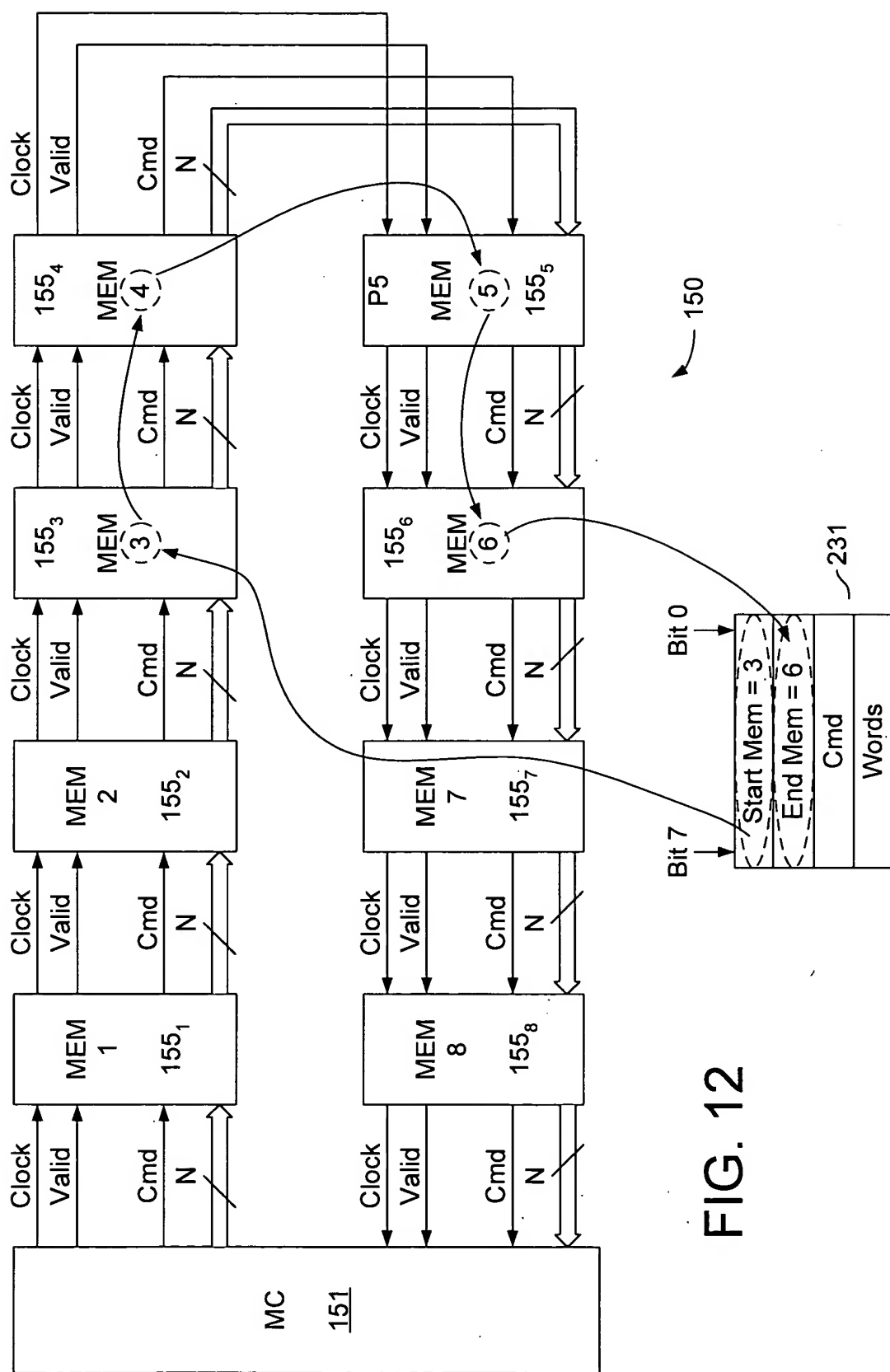


FIG. 12

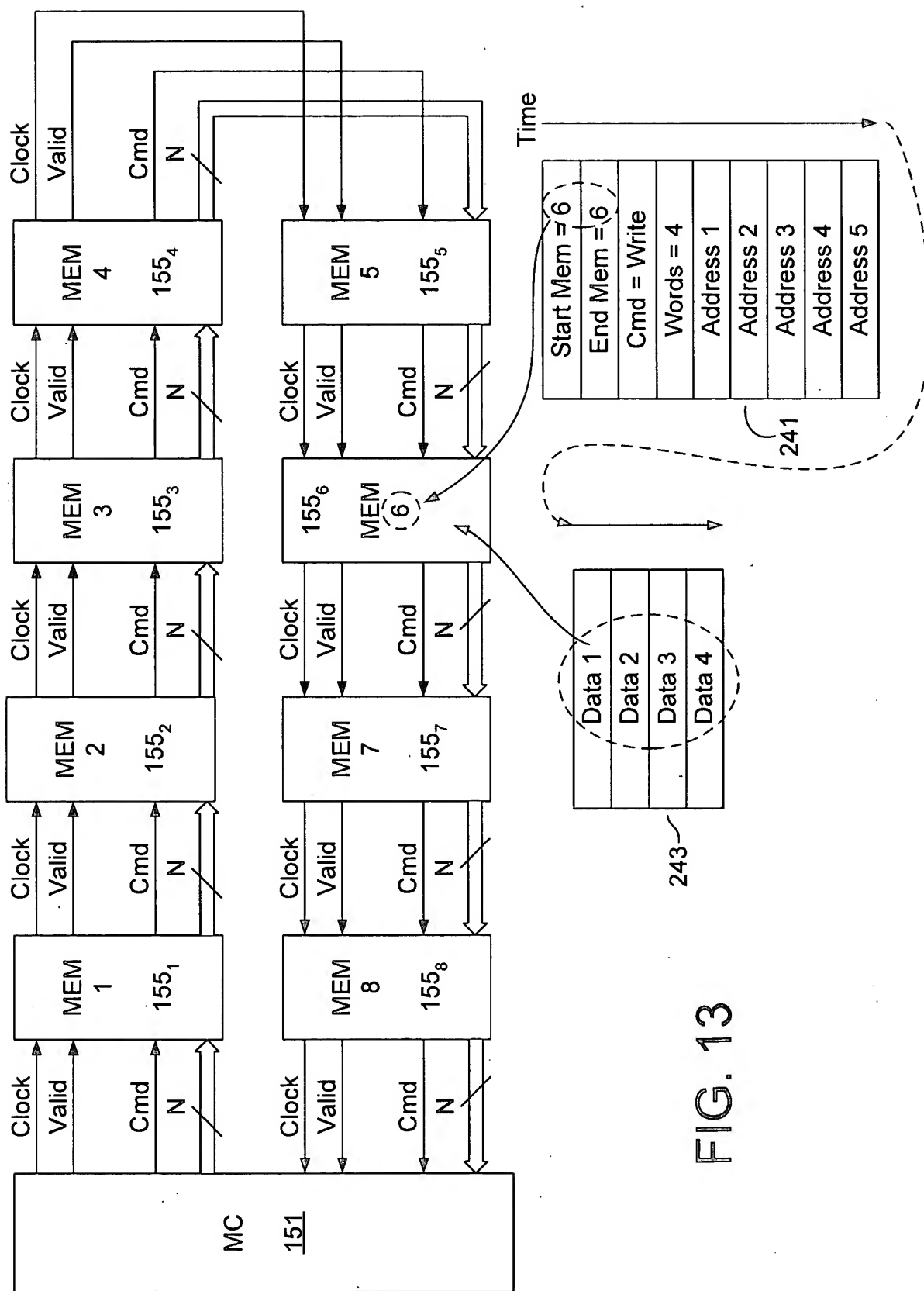


FIG. 13

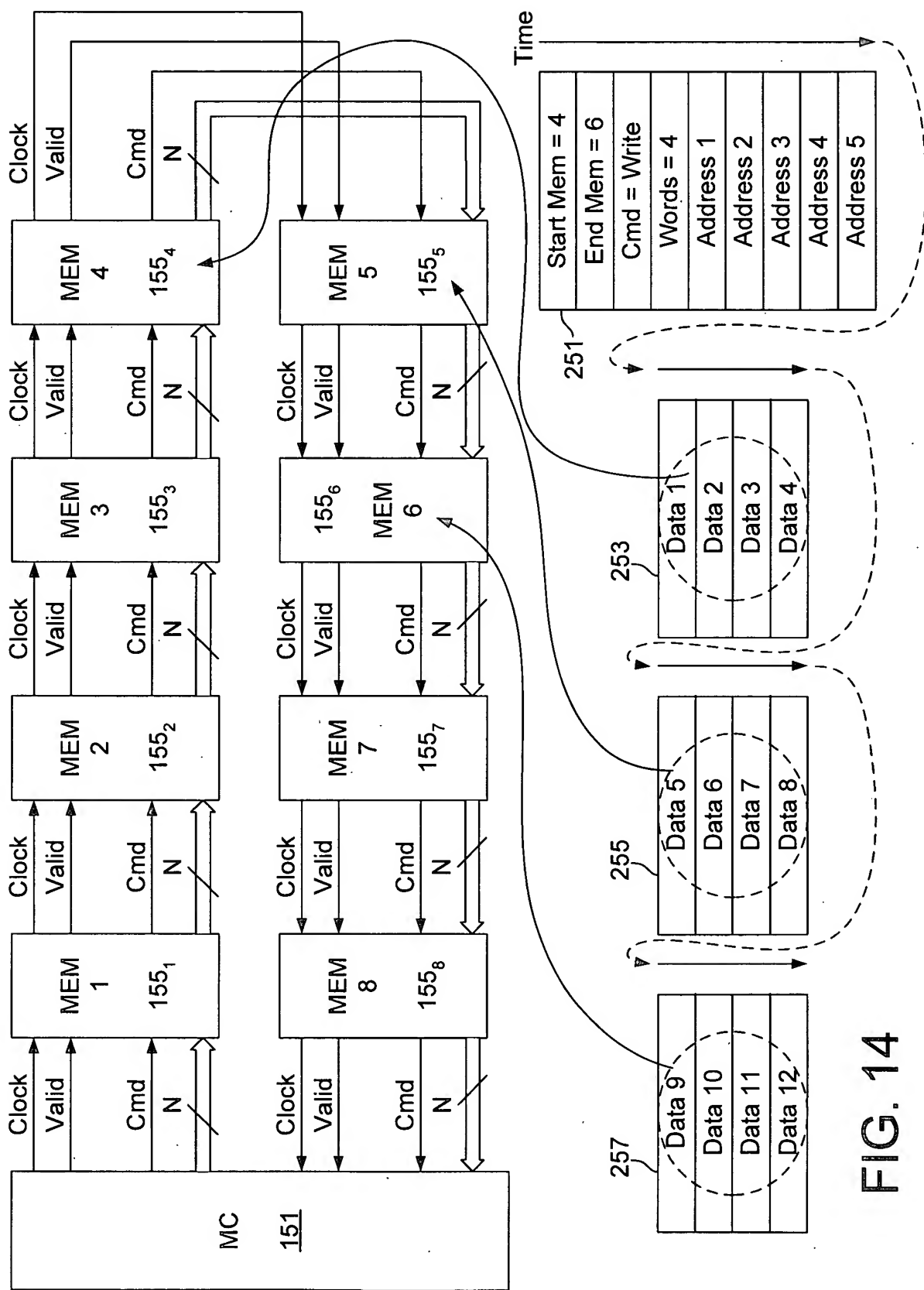


FIG. 14

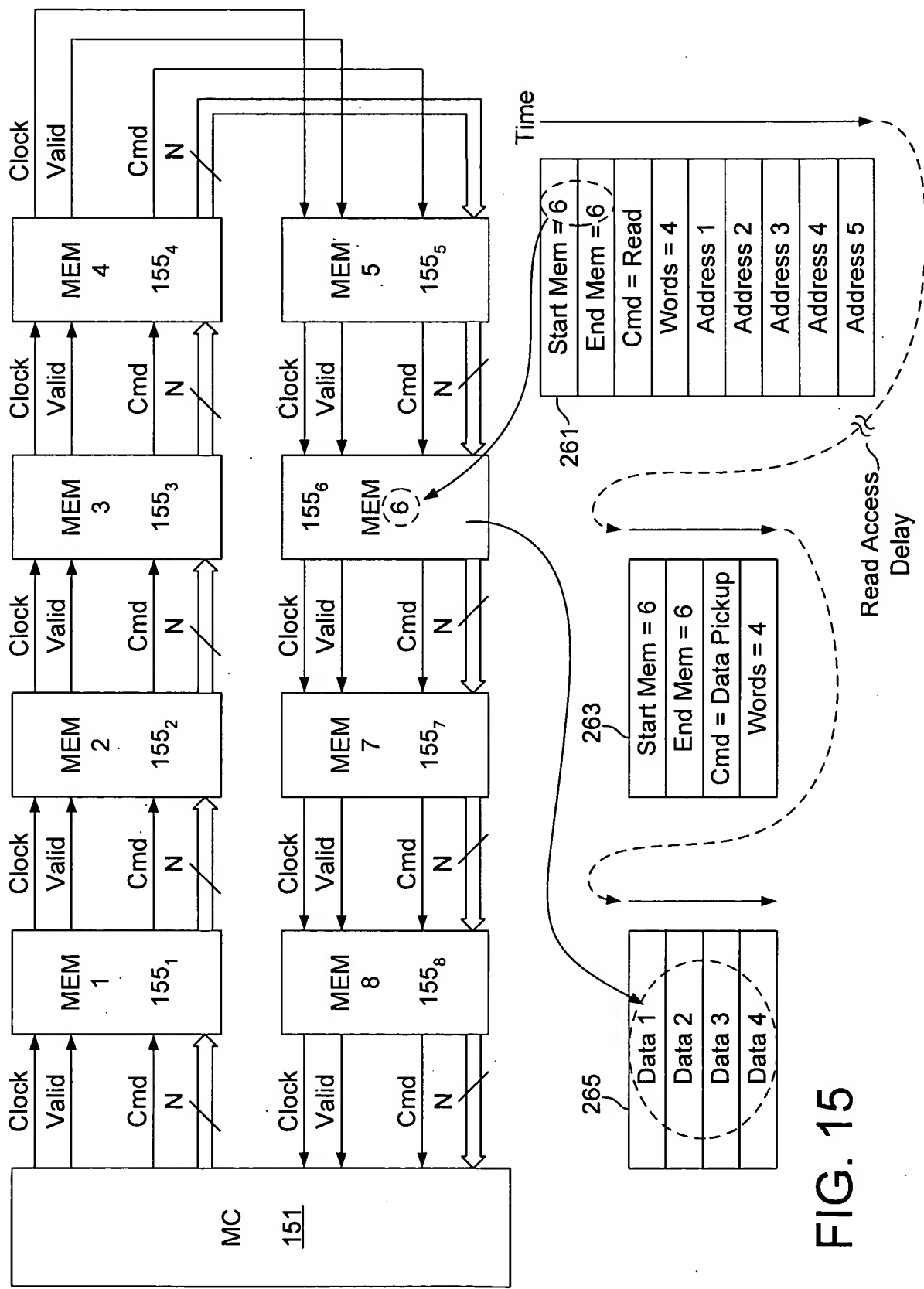


FIG. 15

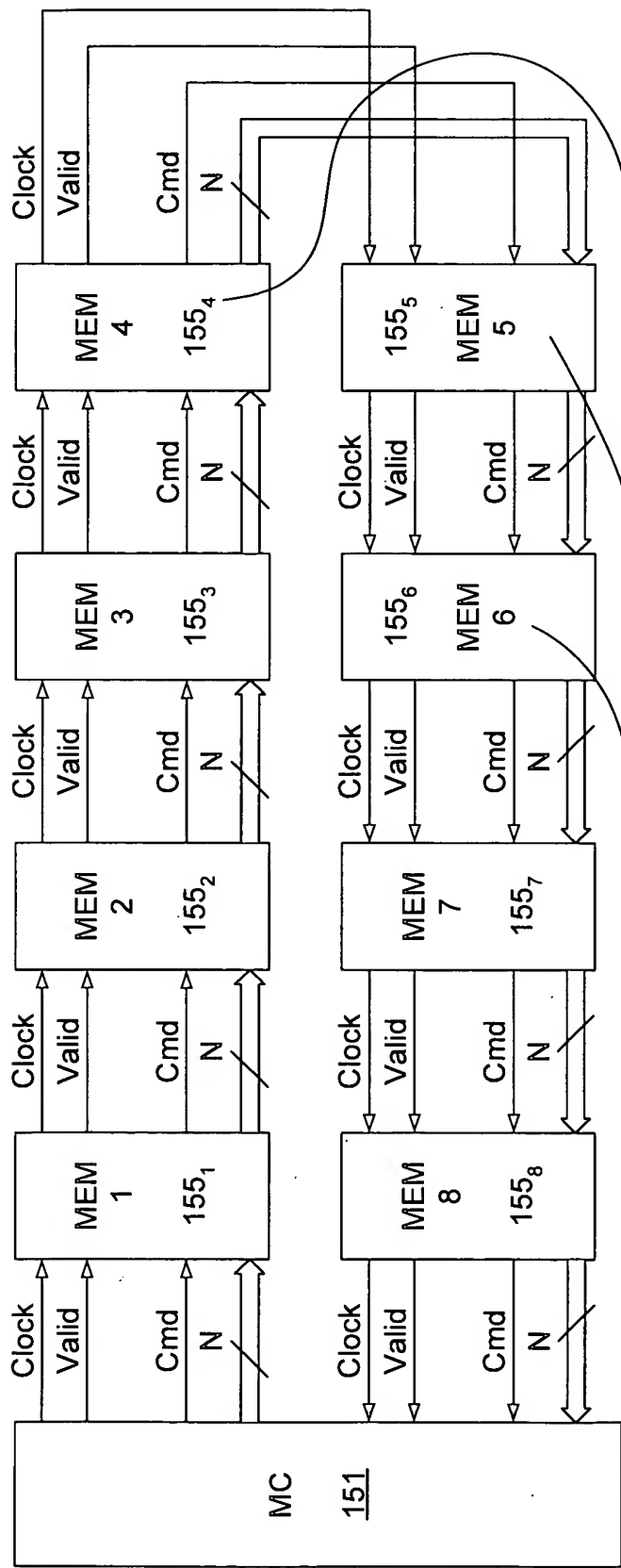
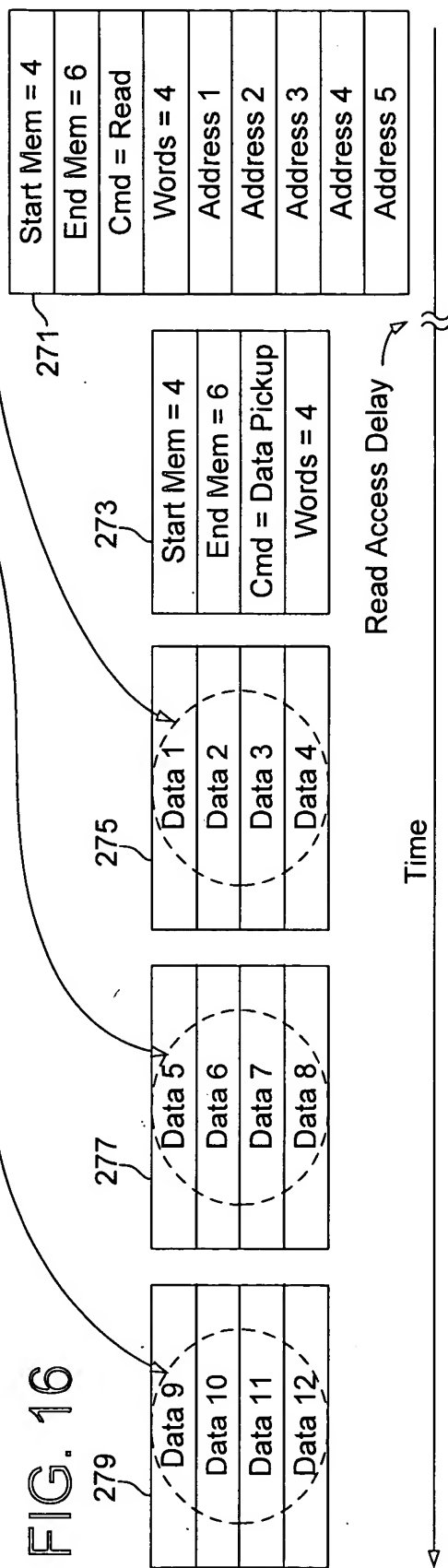
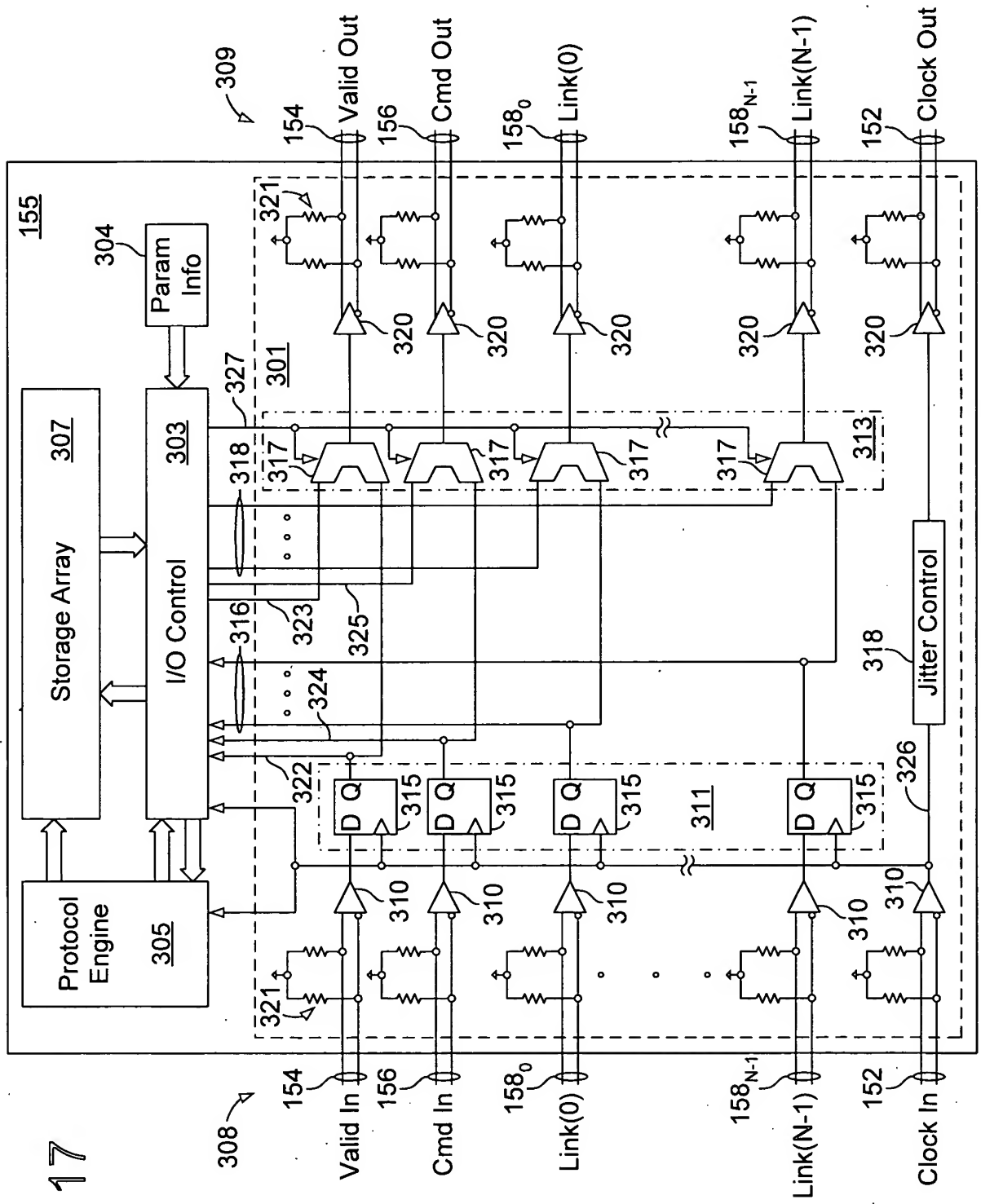


FIG. 16



The diagram illustrates a multi-link system 17. At the top, a Protocol Engine 305 is connected to a Storage Array 307 and an I/O Control block 303. The I/O Control block 303 is also connected to a Param Info block 304. The system includes multiple links, labeled Link(0) through Link(N-1). Each link has a Valid signal (154), a Command signal (156), and a Link signal (158₀ to 158_{N-1}). A Jitter Control block 318 is connected to the Link signals. The system also includes a Clock In signal (152) and a Clock Out signal (152). Various components are shown within dashed boxes 308 and 309, including D flip-flops 315, comparators 310, and multiplexers 317. The diagram shows the internal structure of the I/O Control block 303, including the Jitter Control block 318 and the Link signals 158₀ to 158_{N-1}.



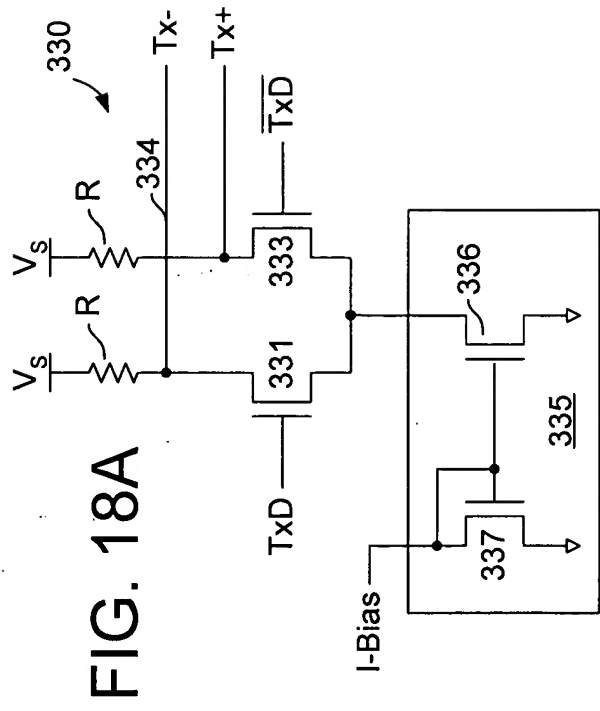
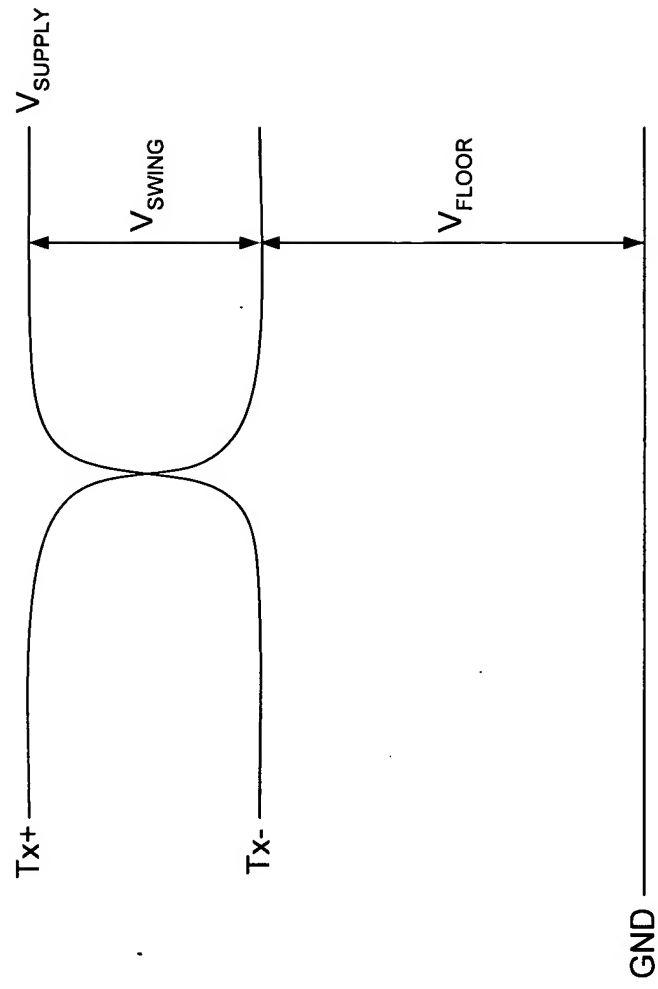


FIG. 18A

FIG. 18B



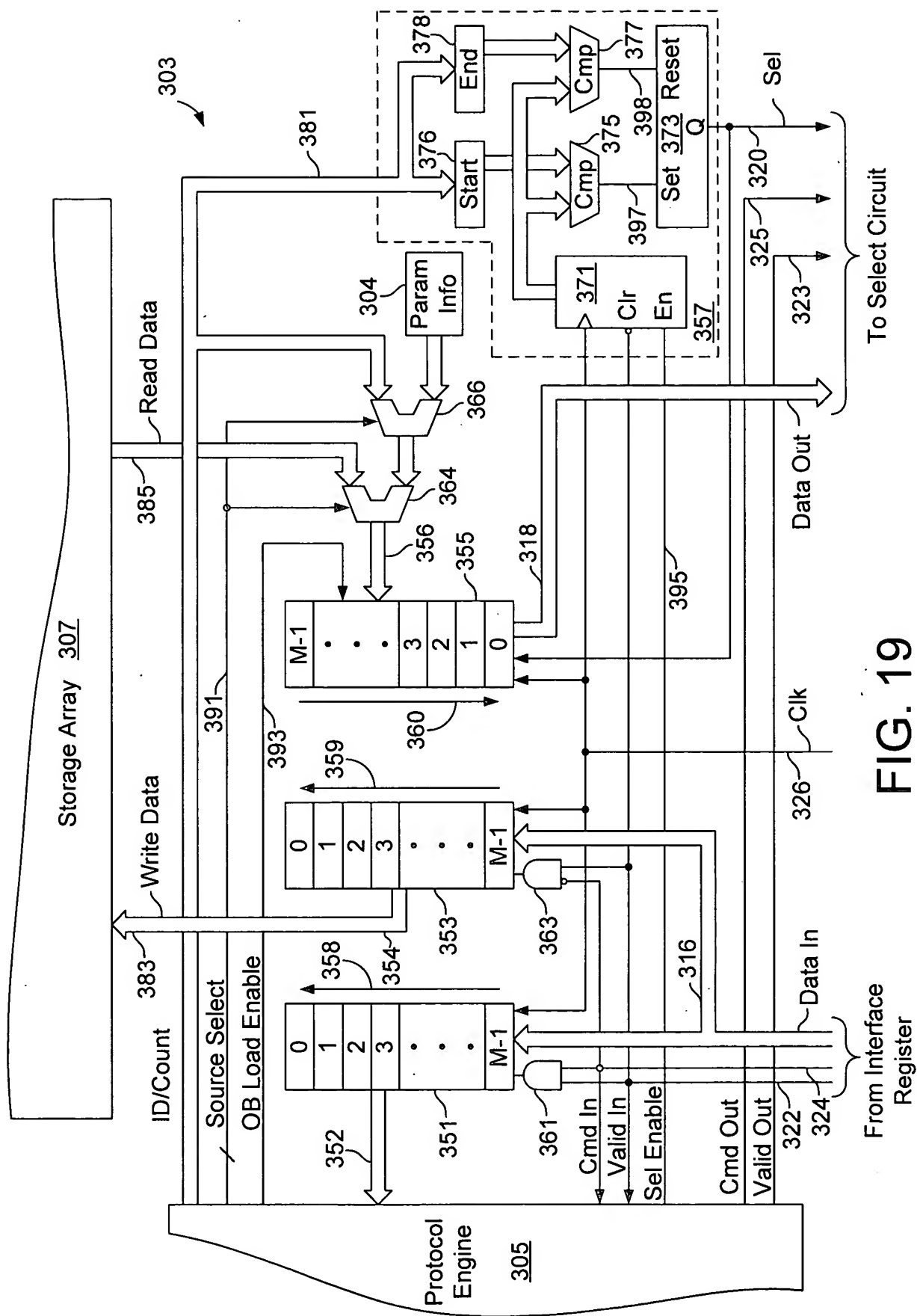
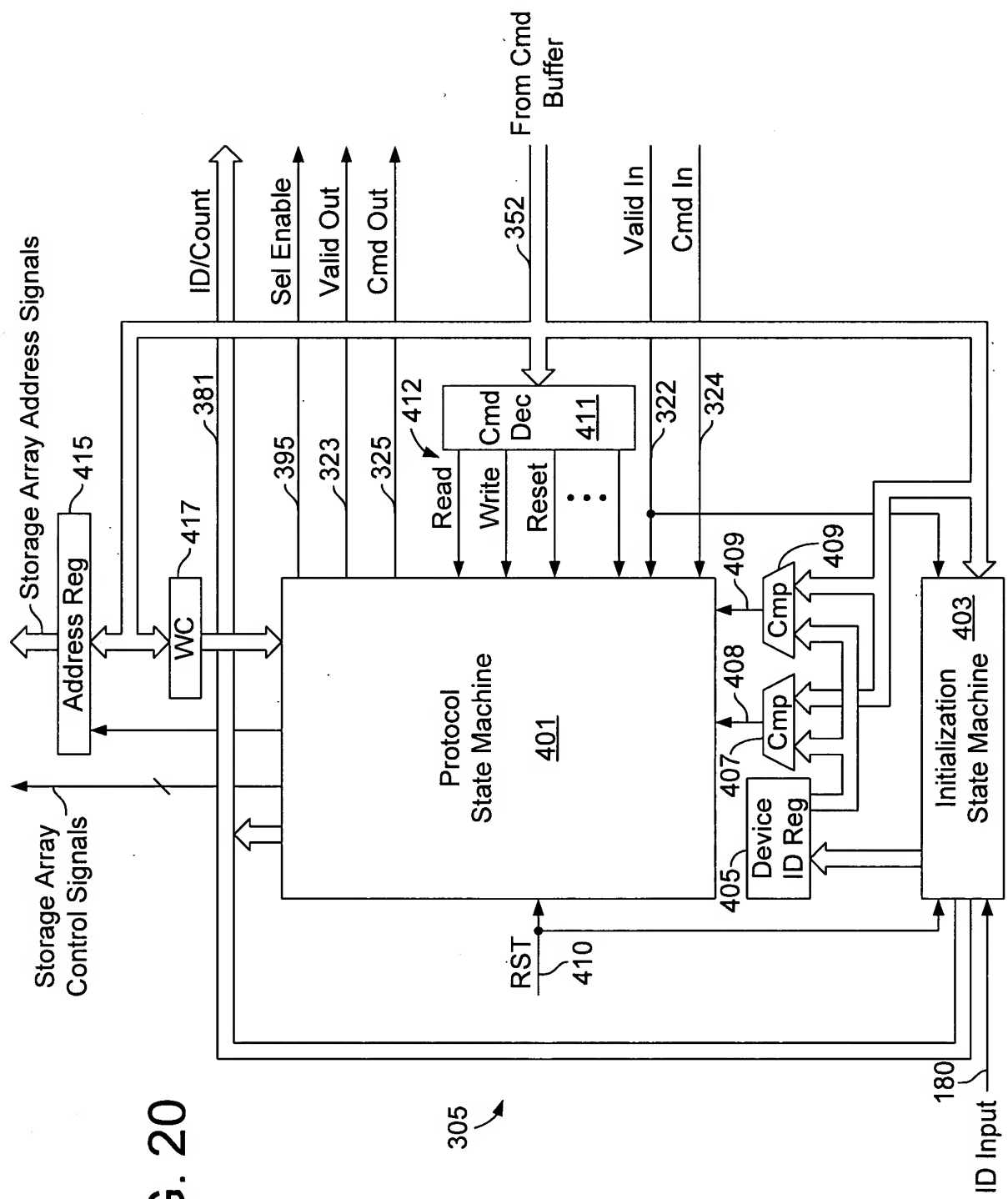


FIG. 19

FIG. 20



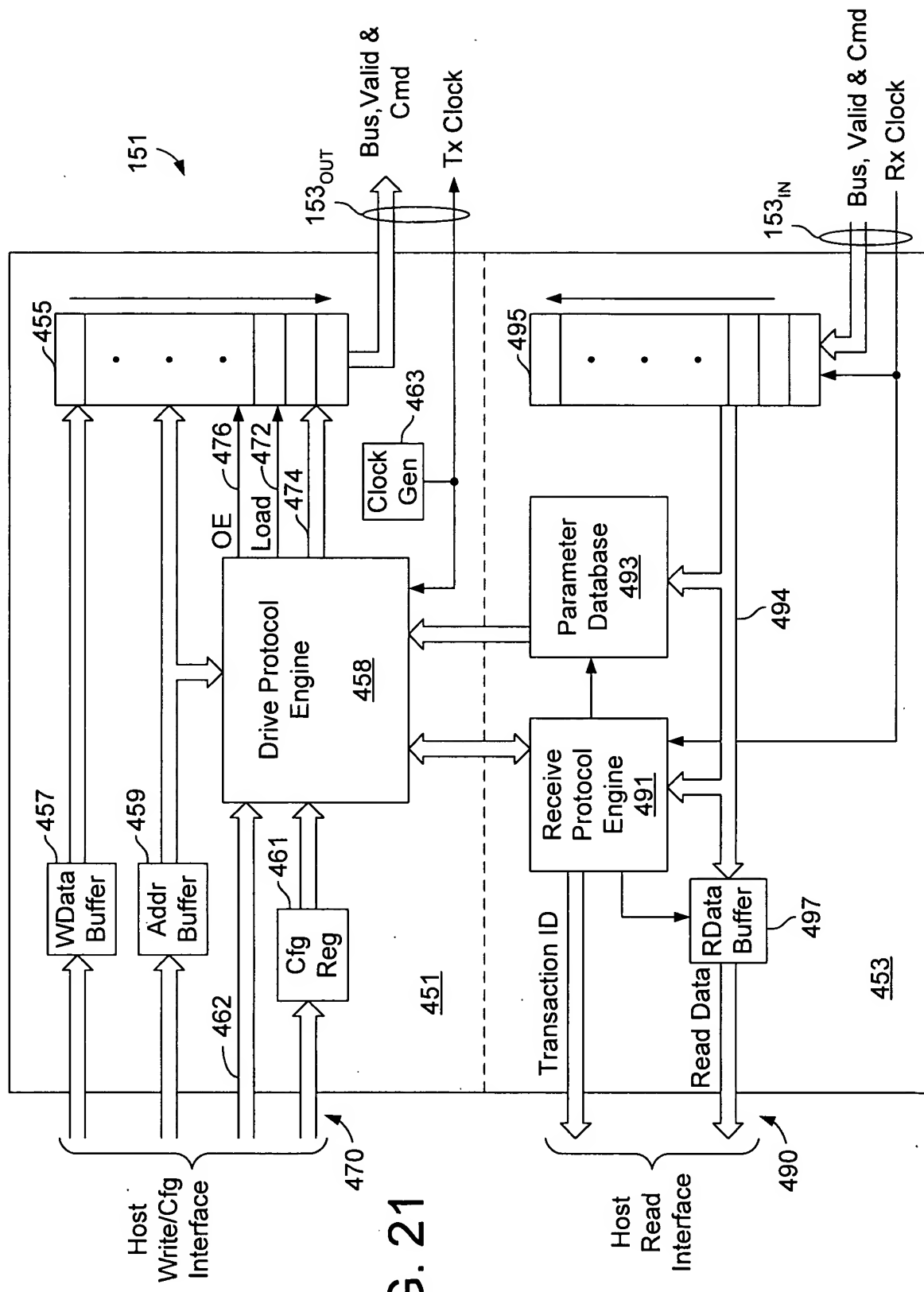


FIG. 21

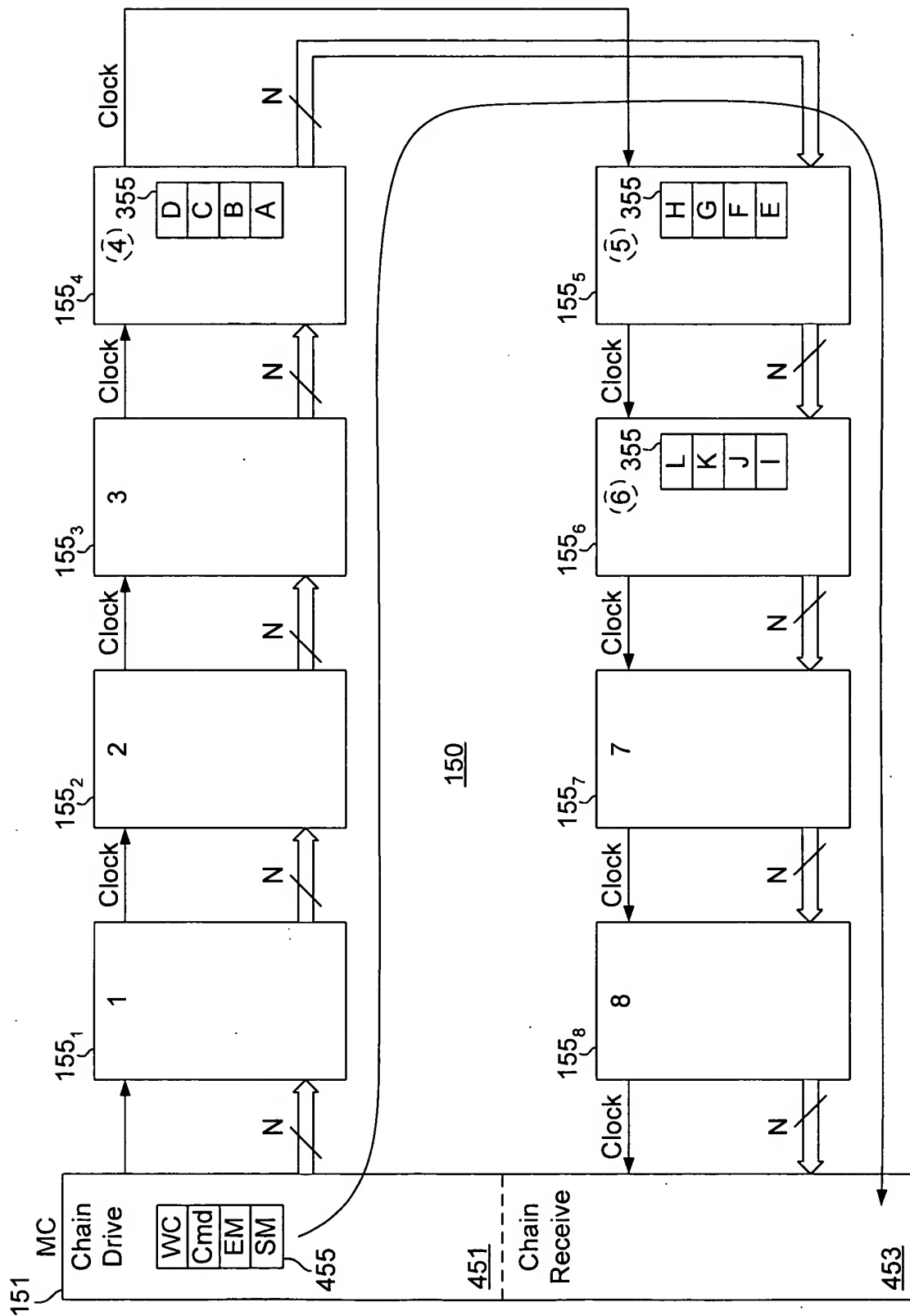


FIG. 22A

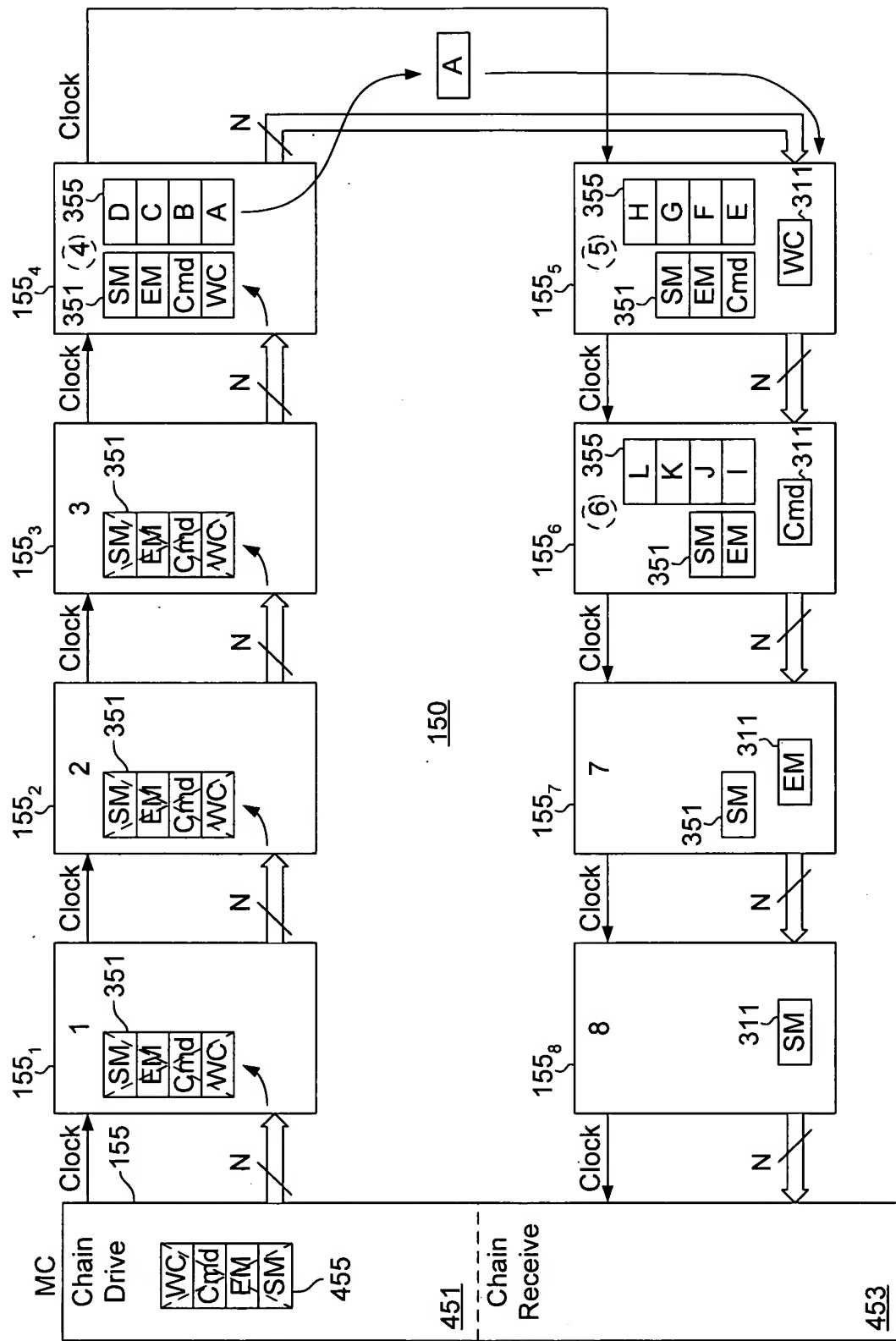


FIG. 22B

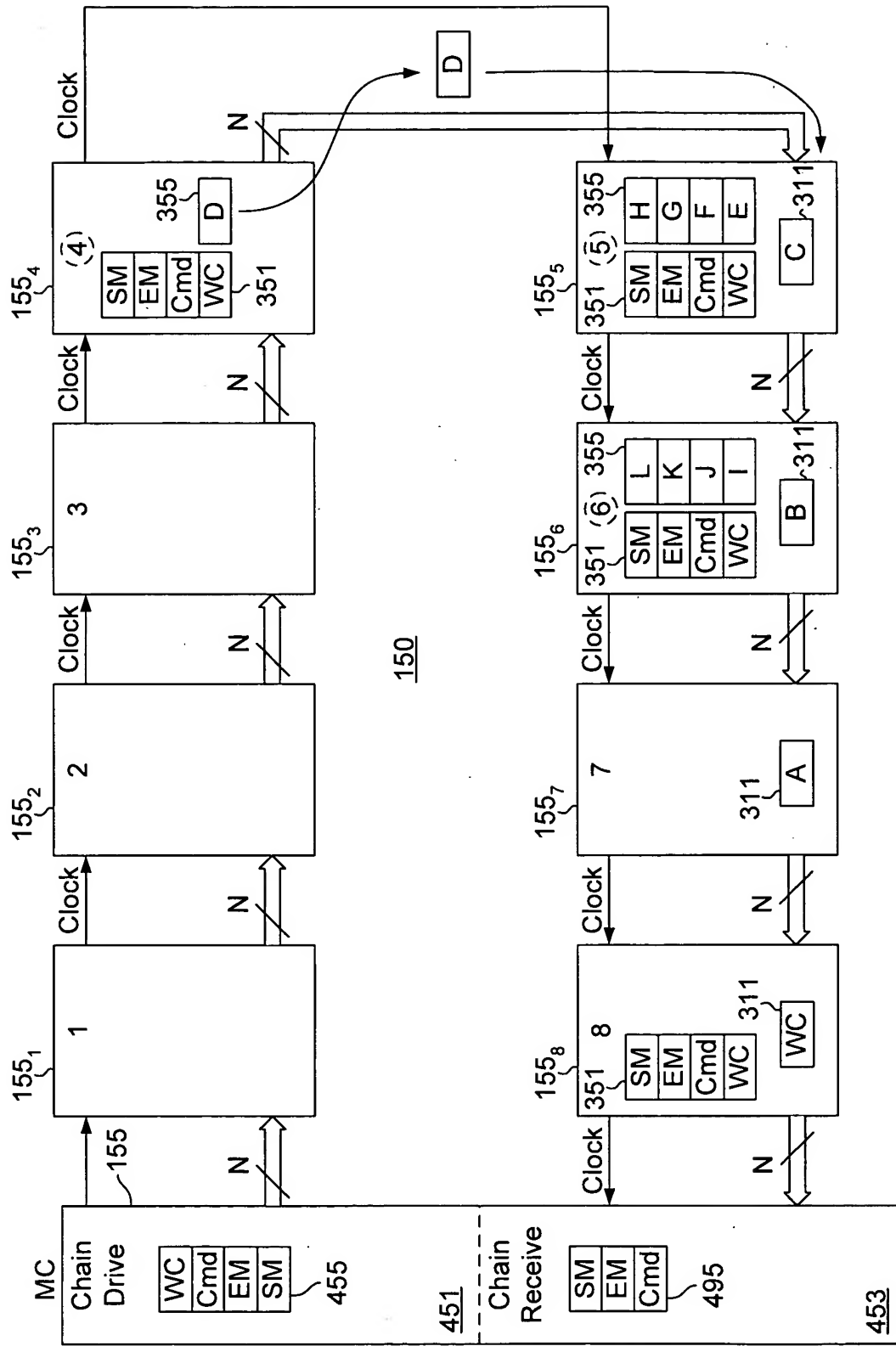


FIG. 22C

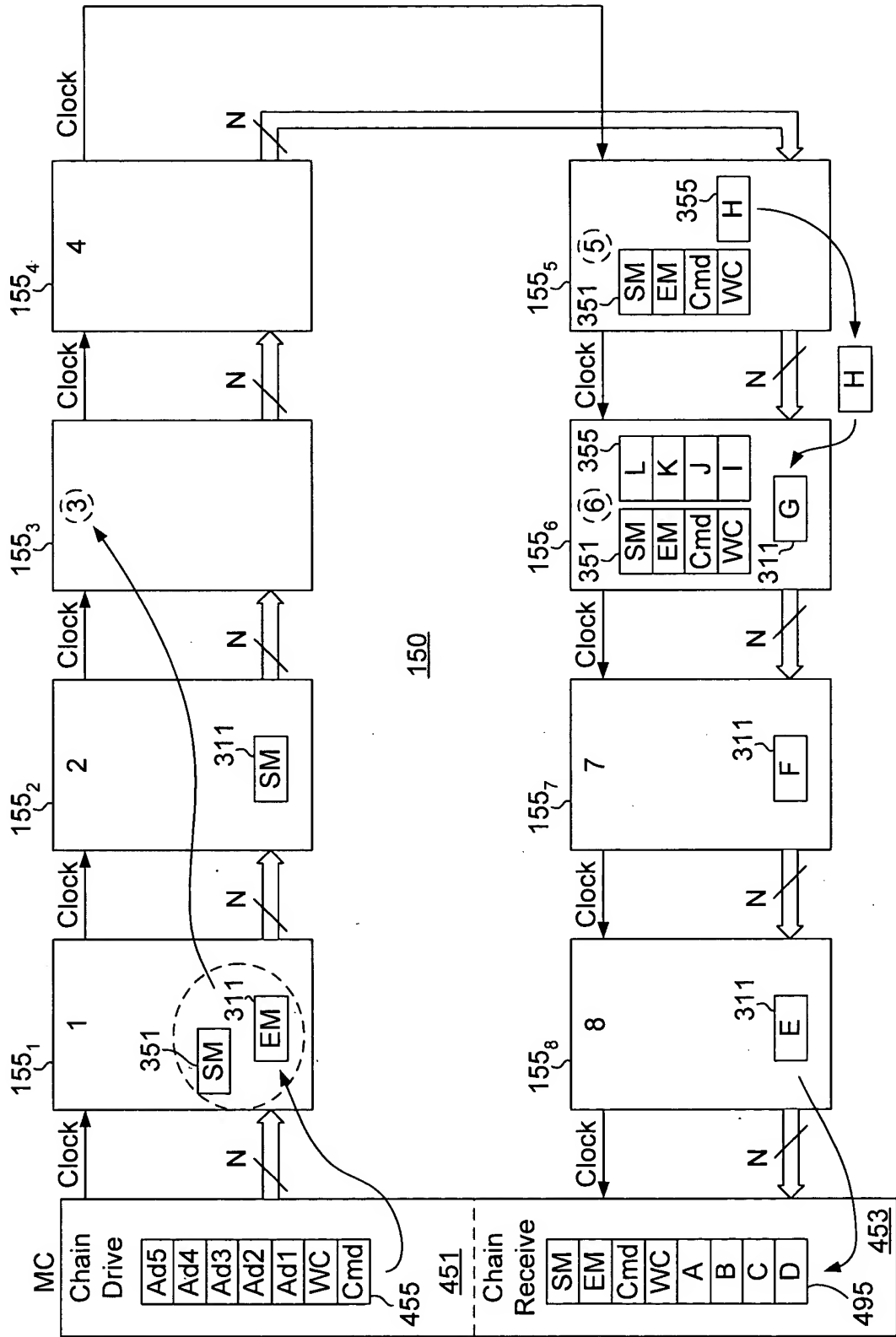
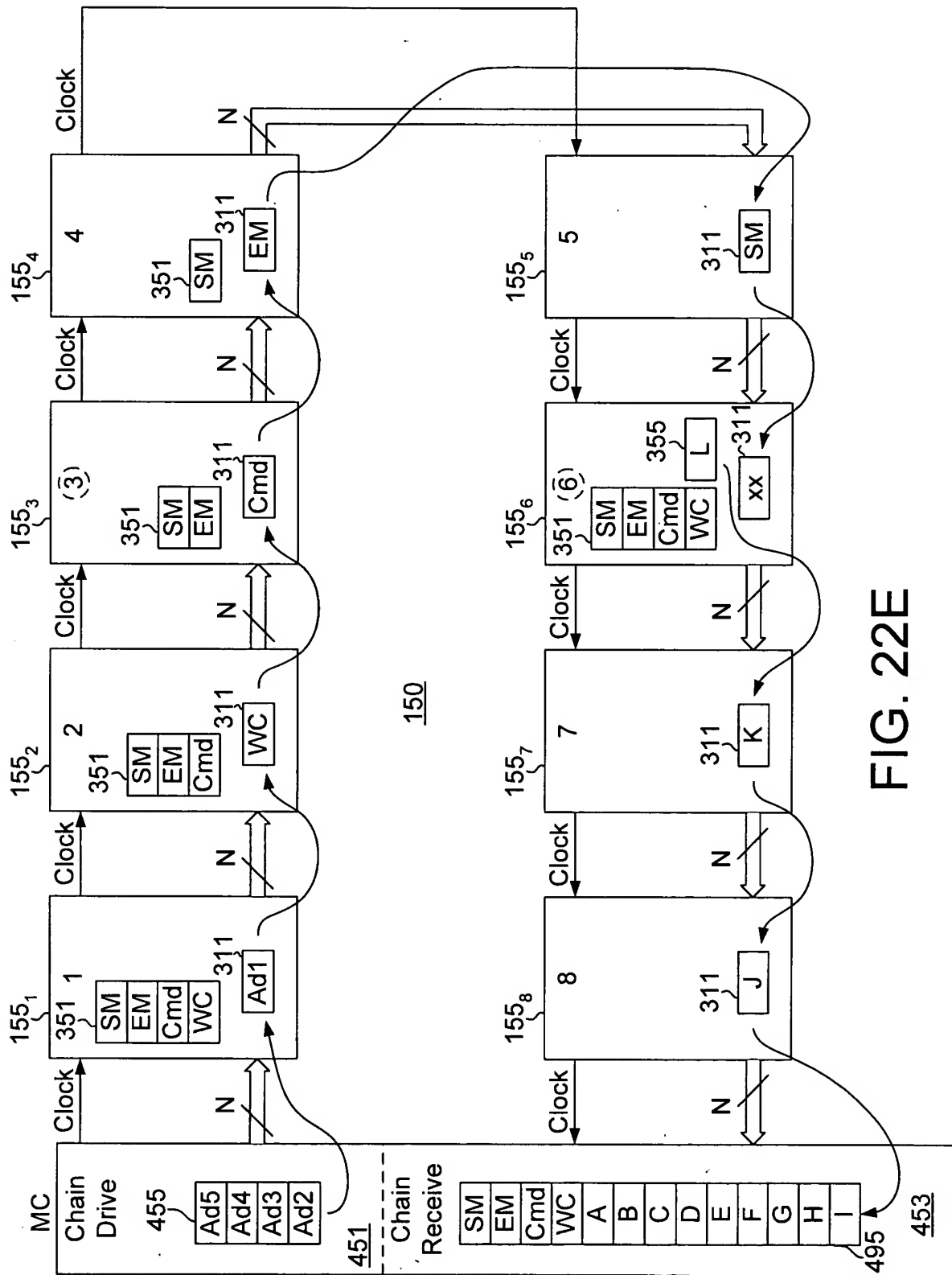


FIG. 22D



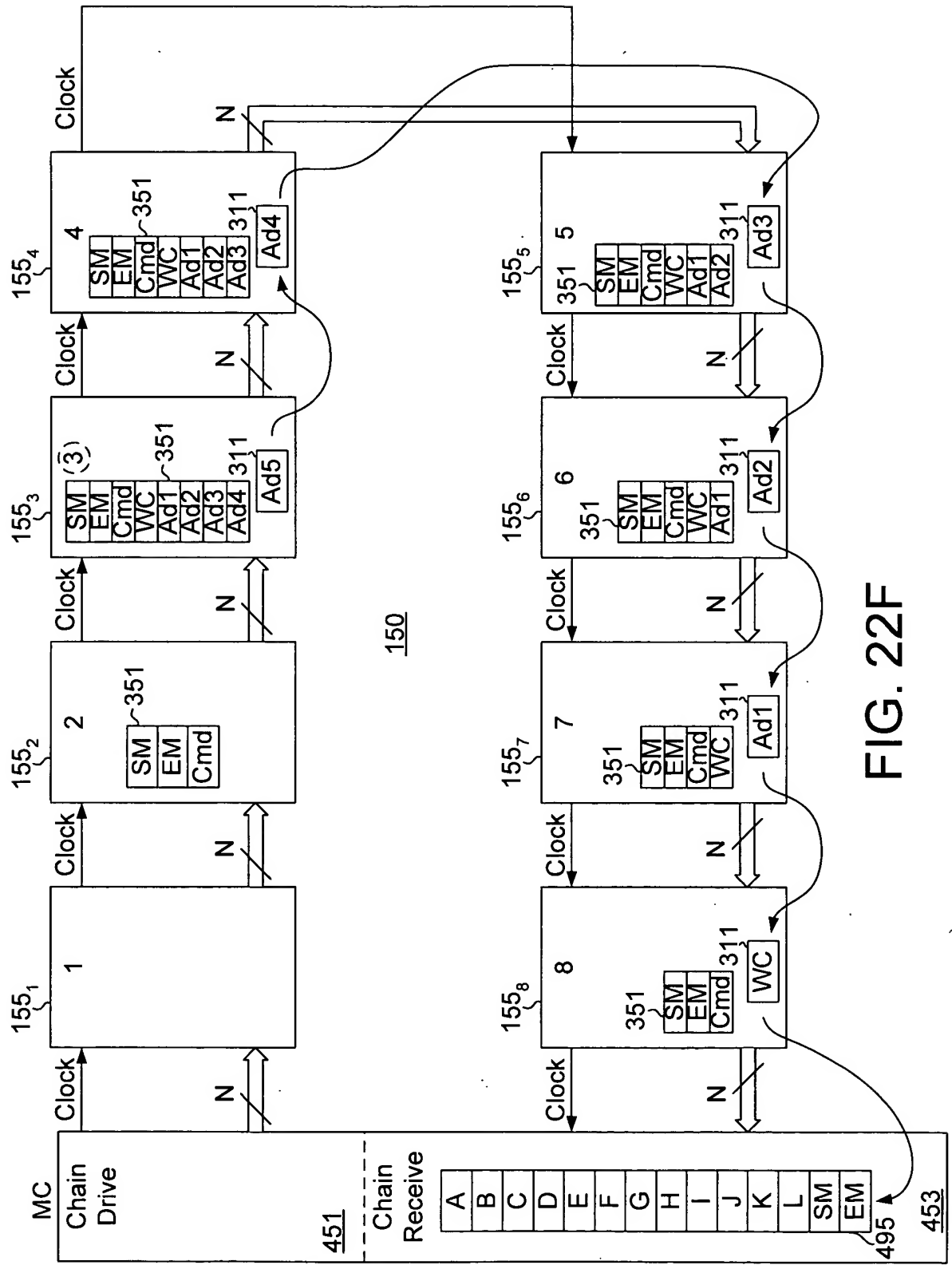


FIG. 22F

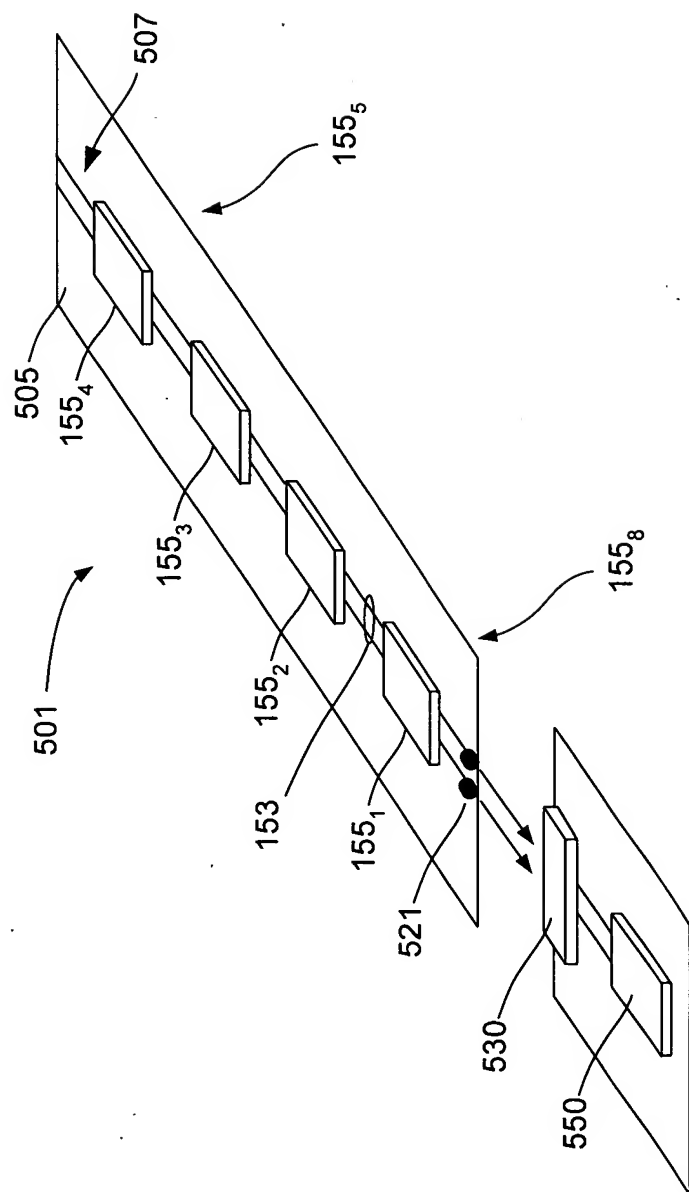


FIG. 23